Rajeev Gandhi Memorial College of Engineering and Technology,
Nandyal (Autonomous)

Department of Electronics and Communication Engineering

COURSE FILE

ACADEMIC YEAR : 2022-23
SUBJECT : VLSI DESIGN
DEPARTMENT : Electronics & Communication Engineering
FACULTY NAME : Dr.C.Venkataiah

Dr. Kethepalli Mallikarjuna
HOD of ECE

Dr. KETHEPALLI MALLIKARJUNA
B.E, M.Tech, PhD, MISTE, FIETE, MIE
Professor & HOD
Department of ECE
RGM College of Engg. & Tech. (Autonomous)
NANDYAL - 518 501, Kurnool (Dist), A.P.

Dr.T.Jayachandra prasad
Principal

Dr. T. JAYACHANDRA PRASAD
M.E,Ph.D.,
PRINCIPAL
R G M College of Engg. & Tech.,
(Autonomous)
NANDYAL-518 501, Nandyal (Dt), A.P.

R.G.M.COLLEGE OF ENGINEERING & TECHNOLOGY, NANDYAL – 518 501
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

IV B.Tech., I-Semester **Academic Year: 2022-23**
w.e.f: 01-08-2022
A-Section : Rotation B-Section : Rotation
C-Section : RB-2140 D-Section : RB-2150

Period/ Day	Section	1 9.00 AM To 9.50 AM	2 9.50 AM To 10.40 AM	3 11.00 AM To 11.50 AM	4 01.00 PM To 01.50 PM	5 1.50 PM To 2.40 PM	6 2.40 PM To 3.30 PM	7 3.30 PM To 4.20 PM
MON	A	DIP	MEFA	MW&OC	DDV	MW&OC Lab/DSP&IP Lab		
	D	VLSID	MEFA	VLSID	DIP	MW&OC	DDV	COU
	B	MW&OC Lab/DSP&IP Lab			DIP	MW&OC	MEFA	LIB
	C	DDV	COU	IE/ISTE	VLSID	DIP	VLSID	MW&OC
TUE	A	VLSID	MEFA	LIB	COU	Mini Project-II		
	D	MW&OC Lab/DSP&IP Lab			MW&OC	MEFA	DIP	VLSID
	B	MW&OC	DDV	MEFA	DIP	VLSID	IEI/ISTE	VLSID
	C	VLSID	DIP	MEFA	MW&OC	MW&OC Lab/DSP&IP Lab		
WED	A	MW&OC Lab/DSP&IP Lab			MEFA	DIP	MW&OC	DDV
	D	MW&OC	DDV	LIB	MEFA	VLSID	MW&OC	DIP
	B	DIP	MEFA	MW&OC	VLSID	DDV	DIP	MW&OC
	C	VLSID	MEFA	DIP	MW&OC	Mini Project-II		
THU	A	MW&OC	DIP	MEFA	VLSID	VLSID	MW&OC	DIP
	D	DDV	MW&OC	DIP	DIP	Mini Project-II		
	B	MW&OC Lab/DSP&IP Lab			VLSID	DDV	MEFA	DIP
	C	VLSID	MEFA	LIB	MW&OC	DIP	MW&OC	DDV
FRI	A	VLSID	MEFA	MW&OC	DIP	DDV	VLSID	IEL/ISTE
	D	DIP	MEFA	VLSID	DDV	MW&OC Lab/DSP&IP Lab		
	B	VLSID	COU	MEFA	MW&OC	Mini Project-II		
	C	MW&OC Lab/DSP&IP Lab			DDV	DIP	MEFA	VLSID
SAT	A	DDV	DIP	VLSID	MW&OC	Main Project Phase-I		
	D	VLSID	MEFA	MW&OC	IEI/ISTE			
	B	DIP	VLSID	MW&OC	DDV			
	C	MW&OC	DIP	DDV	MEFA			

Subject	Section	Name of the Faculty
MW&OC	A	Mr.K.Anil Kumar
VLSID	A	Smt.M.Dhana Lakshmi
DIP	A	Mr.Y.Madhu Sudhana Reddy
MEFA	A	Mr.K.Rama Krishna
DDV	A	Mr.J.Leela Mahendra Kumar
MW&OC Lab	A	**Mr.KAK**/Dr.JSP/BS
DSP&IP Lab	A	**Mr.YMSR**/Smt.RS/KMV
MP-II	A	Dr.JSP/VS/PAR/MP
Counselling	A	Mr.K.Anil Kumar
IEI/ISTE	A	Smt.V.Saraswathi

Subject	Section	Name of the Faculty
MW&OC	B	Smt.R.Madhavi
VLSID	B	Smt.M.Maheswari
DIP	B	Mr.P.Dinesh
MEFA	B	Mr.K.Rama Krishna
DDV	B	Mr.P.Rangappa
MW&OC Lab	B	**Mr.SKNB**/Mr.SKH/MDL
DSP&IP Lab	B	**Mr.PR**/Mr.NNK/PD
MP-II	B	Dr.JSP/PAR/MP/RM
Counselling	B	Mr.K.Anil Kumar
IEI/ISTE	A	Smt.V.Saraswathi

Subject	Section	Name of the Faculty
MW&OC	C	Mr.S.Khasim Noor Basha
VLSID	C	Smt.B.Swetha
DIP	C	Mr.N.Naga Raja Kumar
MEFA	C	Mrs.S.Haritha
DDV	C	Mr.P.Rangappa
MW&OC Lab	C	**Mr.SKH**/Mr.SKNB/MDL
DSP&IP Lab	C	**Mr.NNK**/Mr.PR/PD
MP-II	C	Mr.PM/MP/LU/RM
Counselling	C	Mr.M.V.Raja Sekar
IEI/ISTE	A	Smt.V.Saraswathi

Subject	Section	Name of the Faculty
MW&OC	D	Mr.V.Raja Sekar
VLSID	D	Dr.C.Venkataiah
DIP	D	Mr.K.Masthan Vali
MEFA	D	Mr.Y.Mallikarjuna Achari
DDV	D	Mr.J.Leela Mahendra Kumar
MW&OC Lab	D	**Mr.MVRS**/Mr.KAK/BS
DSP&IP Lab	D	**Smt.RS**/Mr.YMSR/KMV
MP-II	D	LU/PAR/RM/YPS
Counselling	D	Mr.M.V.Raja Sekar
IEI/ISTE	A	Smt.V.Saraswathi

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(A0426157) VLSI DESIGN

OBJECTIVES:

- To know the fabrication process of CMOS technology and its layout design rules
- To study the concepts of CMOS inverters and their sizing methods
- To understand basic circuit concepts and designing Arithmetic Building Blocks.
- To have an overview of Low power VLSI.
- To know the concepts of power estimation and delay calculations in CMOS circuits.

OUTCOMES:

- Understand and calculate device and circuit parameters of MOSFET.
- Draw the Stick diagram and Layout diagrams for nMOS/CMOS circuits.
- Design basic logic functions with different logic styles and compare various logic design styles on their performance metrics.
- Study the importance of low power design and basic techniques for low power design.
- Impart the research skills and encourage continuous learning in the area of microelectronics and VLSI design.

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2											2		
CO2		2	3											1	
CO3	1	1	3												2
CO4						3	2						2		
CO5											2	3			2

UNIT I

INTRODUCTION : Introduction to IC Technology – MOS, PMOS, NMOS, CMOS technologies Oxidation, Lithography, Diffusion, Ion implantation, Metallization, Encapsulation, Integrated Resistors and Capacitors, types of packages sets significance.

UNIT II

BASIC ELECTRICAL PROPERTIES: Basic Electrical Properties of MOS Circuits: Enhancement mode transistor action, $I_{ds}V_{ds}$ relationships, MOS transistor threshold Voltage, g_m, g_{ds}; Pass transistor, Inverter with ntype MOSFET Load, Enhancement load NMOS, Depletion Load NMOS, CMOS Inverter analysis and design, BiCMOS Inverters.

UNIT III

VLSI CIRCUIT DESIGN PROCESSES: MOS Layers, Stick Diagrams, Design Rules and Layout: Lambda based CMOS Design rules for wires, Contacts and Transistors.Layout Diagrams for NMOS and CMOS Inverters and Gates.

UNIT IV

BASIC CIRCUIT CONCEPTS: Sheet Resistance R_S and its concept to MOS, Area Capacitances of layers, standard unit of capacitance Cg, area capacitance calculations, The Delay unit, Inverter delays, estimation of CMOS inverter delay, Wiring Capacitances, Choice of layers.

UNIT V

SHORT CHANNEL EFFECTS AND DEVICE MODELS: Scaling Theory, Threshold voltage variation, Mobility Degradation, Velocity Saturation, Hot Carrier Effects, Output Impedance Variation with Drain-Source Voltage, MOS Device Models- Level 1, Level 2, Level 3, BSIM Series, Charge and Capacitance Modeling, Temperature Dependence, Process Corners, Analog Design in a Digital World.

UNIT VI

INTRODCTION TO LOW POWER VLSI: Introduction, overview of power consumption,Sources of Power Dissipation, Static Power Dissipation, Active Power Dissipation, low power design through voltage scaling, estimation and optimization of switching activity.

TEXTBOOKS:

1. Essentials of VLSI circuits and systems – Kamran Eshraghian, EshraghianDougles and A. Pucknell, PHI, 2005 Edition.
2. CMOS digital integrated circuits analysis and design by SungMo Kand and Yusuf Leblebici, Tata McGraw Hill, 3rd edition.

REFERENCES:

1. Introduction to VLSI Circuits and Systems John .P. Uyemura, JohnWiley, 2003.
2. Modern VLSI Design Wayne Wolf, Pearson Education, 3rd Edition, 1997.
3. VLSI Technology – S.M. SZE, 2nd Edition, TMH, 2003.
4. Principles of CMOS VLSI Design Weste and Eshraghian, Pearson Education, 1999.
5. Digital Integrated Circuits – A design perspective, John M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Pearson Education, 2rd Edition.

RGM COLLEGE OF ENGINEERING & TECHNOLOGY
NANDYAL-518 501
AUTONOMOUS

(ESTD-1995)

LESSON PLAN

Name of the Faculty: Dr. C. VENKATAIAH **Branch & Section: ECE-D**
Subject: VLSI DESIGN **Total No of Hours**:62
Class : IV YEAR **I** SEM **Year: 2022-2023**

Unit No.	Unit	Topic to be covered	No. of hours
I	**INTRODUCTION** (8)	Introduction to VLSI	1
		Introduction to IC Technology -MOS, PMOS, NMOS, CMOS technologies	2
		Oxidation, Lithography, Diffusion, Ion implantation, Metallization, Encapsulation	3
		Integrated Resistors and Capacitors	1
		types of packages sets significance.	1
II.	**BASIC ELECTRICAL PROPERTIES** (10)	I_{ds}-V_{ds} relationships	1
		MOS transistor threshold Voltage, g_m, g_{ds}	1
		Pass transistor	1
		NMOS Inverter,	2
		Various pull ups	2
		CMOS Inverter analysis and design	2
		Bi-CMOS Inverters	1
III	**VLSI CIRCUIT DESIGN PROCESSES** (12)	MOS Layers, Stick Diagrams	2
		Design Rules and Layout	2
		Lambda based CMOS Design rules for wires, Contacts	3
		Transistors Layout Diagrams for NMOS	2
		CMOS Inverters and Gates	3
VI.	**BASIC CIRCUIT CONCEPTS** (10)	Sheet Resistance R_S and its concept to MOS	2
		Area Capacitances of layers	1
		standard unit of capacitance Cg	2
		area capacitance calculations	1
		The Delay unit, Inverter delays	2
		estimation of CMOS inverter delay	1
		Wiring Capacitances, Choice of layers.	1
V.	**SHORT CHANNEL EFFECTS AND DEVICE MODELS** (12)	Scaling Theory	1
		Threshold voltage variation, Mobility Degradation	2
		Velocity Saturation, Hot Carrier Effects, Output Impedance Variation with Drain-Source Voltage	3
		MOS Device Models- Level 1, Level 2, Level 3	3
		BSIM Series, Charge and Capacitance Modeling,Temperature Dependence	2
		Process Corners, Analog Design in a Digital World.	1
VI.	**INTRODCTION TO LOW POWER VLSI** (10)	Introduction	1
		Over view of power consumption	3
		Low power design through voltage scaling	3
		Estimation and optimization of switching activity.	3
	Total		62

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Signature of The Faculty

RGM COLLEGE OF ENGINEERING & TECHNOLOGY

(AUTONOMOUS)

NANDYAL - 518 501. Kurnool (Dist.) A.P.

EDUCATION FOR PEACE

(ESTD-1995)

ATTENDANCE REGISTER

ACADEMIC YEAR	: 2022-23	**SEM**	: I / II
COURSE	: B.Tech	**CLASS :**	IV
BRANCH / SECTION	: ECE-D		
SUBJECT & CREDITS	: VLSI Design		
FACULTY	: Dr. C. Venkataiah		

R.G.M. COLLEGE OF ENGINEERING

ATTENDANCE

Class :

Branch :

Semister / Year

Roll No.	Name	Date											
1409110		1	2	3	4	5	6	7	8	9	10	11	12
401	Ajay Babu.A	P	P	3	A	5	6	7	8	9	A	A	9
402	Ajay Kumar.B	A	A	1	A	3	4	5	6	7	A	9	10
403	AKash MS	A	A	1	2	3	4	5	6	7	8	9	10
420	Bharath Kumar Reddy.A	P	P	3	A	5	6	7	8	9	A	A	9
425	Chaitanya Kumar Reddy.G	A	A	1	2	3	4	5	6	7	8	9	10
427	Chaithanya Reddy.G(PV	A	A	1	2	3	4	5	6	7	A	9	10
435	Dhanush kumar.C	A	A	1	2	3	4	5	6	7	8	9	10
439	Farhan.S	A	A	1	2	3	4	5	6	7	A	A	9
445	Gangasaritha.G	A	A	1	2	3	4	5	6	7	8	9	10
447	Govardhan Reddy.N	A	A	1	2	3	4	5	6	7	8	9	10
449	Guruvardhan Reddy.D	A	A	1	2	3	4	5	6	7	8	9	10
453	Hari Nath.B	A	A	1	2	3	4	5	6	7	8	9	10
458	Hema Sree.D	A	A	1	2	3	4	5	6	7	8	9	10
461	Indra sena.K	A	A	1	2	3	4	5	6	7	A	A	9
465	Jaswanth.G	A	A	1	2	3	4	5	6	7	A	A	9
475	Kiran Kumar.M	A	A	1	2	3	4	5	6	7	A	A	9
484	Lalitha.K	A	A	1	A	2	3	4	5	6	7	8	9
492	Madhu Sudhan Jayanth.P	A	A	1	A	2	3	4	5	6	7	A	9
493	Mahammad Abid Ali.S	A	A	1	2	3	4	5	6	7	8	9	10
496	Mahesh.G	A	A	1	A	2	3	4	5	6	A	A	9
4A3	Manik Basha.D	P	2	3	A	4	5	6	7	8	9	10	11
4B7	Nageraju.T	A	A	1	A	2	3	4	5	6	A	8	9
4C3	Naveen kumar.S	A	A	1	2	3	4	5	6	7	8	A	9
4C7	Nithish kumar.K	A	A	1	2	3	4	5	6	7	8	A	9
4D3	pavan kumar.C	A	A	1	A	2	3	4	5	6	A	A	9
4D4	pavan kumar.P	A	A	1	2	3	4	5	6	7	8	9	10
4D5	pavani.N	A	A	1	2	3	4	5	6	7	8	9	10
4F2	Ram Charan.B	A	A	1	2	3	4	5	6	7	8	9	10
4F4	Rama krishna.N	A	A	1	A	2	3	4	5	6	A	8	9
4F7	Rupendra Reddy.S	A	A	1	2	3	4	5	6	7	A	8	9
Signature of Teacher													
Signature of H.O.D.													
Signature of Principal													

& TECHNOLOGY (Autonomous), NANDYAL.

REGISTER Academic Year from.....to.....Teacher.....

Subject & Credits.....Dept.....

INTERNAL / RECORD MARKS

Roll No.	Assignments 1	Assignments 2	Average (A)	Internal Test 1	Internal Test 2	Internal Marks 75% of MAX	Internal Marks 25%of MIN	Total (I)	Final Internal (I+A)	Remarks
401	10	10		11	09				21	
402	10	10		11	08				21	
403	10	10		12	13				23	
420	10	10		11	09				21	
425	10	10		10	13				23	
427	10	10		15	14				25	
435	10	10		19	15				28	
439	10	10		17	16				27	
445	10	10		11	11				21	
447	8	10		13	12				22	
449	10	10		19	15				28	
453	10	10		12	11				22	
458	10	10		19	17				29	
461	10	10		12	10				22	
465	10	10		15	13				25	
475	10	10		16	15				26	
484	10	10		16	15				26	
492	10	10		17	08				25	
493	10	10		14	14				24	
496	10	10		13	11				23	
4A3	10	10		15	09				24	
4B7	10	10		16	16				26	
4C3	10	10		19	15				28	
4C7	10	10		16	08				24	
4D3	10	10		19	19				29	
4D4	10	10		18	10				26	
4D5	10	10		16	17				27	
4F2	10	10		14	11				24	
4F4	10	10		13	11				23	
4F7	10	10		19	13				28	

R.G.M. COLLEGE OF ENGINEERING

ATTENDANCE

Class :

Branch :

Semister / Year

Roll No.	Name	Date	01/8/22	02/8/22	11/8/22	12/8/22	13/8/22	24/8/22	25/8/22	26/8/22	27/8/22	29/8/22	29/8/22	16/8/22
1 1 5 0 9 1 A 0			1	2	3	4	5	6	7	8	9	10	11	12
4G5	Sai Prasanna. S		A	A	1	A	2	3	4	5	6	7	8	9
4G6	Sai Sahithi. V		A	A	1	A	2	3	4	5	6	7	8	9
4H0	Sai Hemanth. S		A	A	1	A	2	3	4	5	6	7	A	8
4H1	Saikrishna. P		A	A	1	A	2	3	4	5	6	7	A	8
4H6	Sameer. S		A	A	1	A	2	3	4	5	6	7	A	8
4H9	Sandeep kumar. M		A	A	1	2	3	4	5	6	7	8	A	9
4J0	Santhoshini Rupadevi. P		A	A	1	2	3	4	5	6	7	8	9	10
4J1	Saritha. L		A	A	1	A	2	3	4	5	6	7	8	9
4J3	Shahensha. K		A	A	1	A	2	3	4	5	6	7	A	8
4J9	Siva. B		A	A	1	2	3	4	5	6	7	8	9	10
4K3	Sowmya. D		A	A	1	A	2	3	4	5	6	7	A	8
4K9	Sudhamani. D		A	A	1	2	3	4	5	6	7	8	9	10
4M6	Sundaresh. K		A	A	1	2	3	4	5	6	7	8	A	9
4M7	Sunil. D		A	A	1	A	2	3	4	5	6	7	A	8
4N0	Surendra Babu. G		A	A	1	2	3	4	5	6	7	8	A	9
4N8	Syed Basha. S.K		A	A	1	A	2	3	4	5	6	7	8	9
4P5	Vamsikrishna. M		A	A	1	2	3	4	5	6	7	8	A	9
4P6	Vamsi. M		A	A	1	A	2	3	4	5	6	7	A	8
4P9	Varunkumar Reddy. V		A	A	1	A	2	3	4	5	6	7	A	8
4Q7	Venkata Siva Sainath. P		P	P	3	A	4	5	6	7	8	9	A	10
4Q8	Venkateswarlu. P		A	A	1	A	2	3	4	5	6	7	A	8
4Q9	Venkateswarlu. S		A	A	1	2	3	4	5	6	7	8	A	9
4R3	Vinay kumar. B		A	A	1	2	3	4	5	6	7	8	A	9
4R9	Viswasai. P		A	A	1	2	3	4	5	6	7	8	A	9
2 0 0 9 5 A 0 4 0 2	Chetan. S		A	A	1	2	3	4	5	6	7	8	A	9
404	Gangothri. M		A	A	1	A	2	3	4	5	6	7	A	A
407	John Kennedi. G		A	A	1	2	3	4	5	6	7	8	A	A
411	Naga Sekhar Reddy. C		A	A	1	2	3	4	5	6	7	8	A	A
414	Sai kumar Naik. P		A	A	1	2	3	4	5	6	7	8	9	A
418	Shankar. G		P	P	3	A	4	5	6	7	8	9	A	A
Signature of Teacher														
Signature of II.O.D.														
Signature of Principal														

& TECHNOLOGY (Autonomous), NANDYAL.

REGISTER Academic Year from.....to.....Teacher.....

Subject & Credits.....Dept.....

INTERNAL / RECORD MARKS

Roll No.	Assignments 1	Assignments 2	Assignments Average (A)	Internal Test 1	Internal Test 2	Internal Marks 75% of MAX	Internal Marks 25% of MIN	Internal Marks Total (I)	Final Internal (I+A)	Remarks
4GS	10	10		19	12				28	
4G6	10	10		16	08				24	
4H0	10	10		17	08				25	
4H1	10	10		16	07				24	
4H6	10	10		16	13				26	
4H9	10	10		14	11				24	
4J0	10	10		10	09				20	
4J1	10	10		14	13				24	
4J3	10	10		14	10				23	
4J9	10	10		16	08				24	
4K3	10	10		16	13				26	
4K9	10	10		18	15				28	
4M6	8	10		14	09				22	
4M7	10	10		17	10				26	
4N0	10	10		17	A				23	
4N8	10	10		16	11				25	
4P5	8	10		11	09				20	
4P6	10	10		04	14				22	
4P9	10	10		10	07				20	
4Q7	10	10		16	16				26	
4Q8	10	10		16	10				25	
4Q9	10	10		12	A				19	
4R3	8	10		14	19				27	
4R5	8	10		11	05				19	
2009CA0402	10	10		13	10				23	
406	10	10		18	18				28	
407	10	10		17	13				26	
411	10	10		19	13				28	
414	10	10		16	11				25	
418	10	10		14	13				24	
	##	##		##	##				##	

LECTURE RECORD

Subject : VLSI Design. Total Exams.....

Credits : Each for.....hrs.

Internal Mid Exam Marks : Total quizes

Internal Quiz Marks : No. of Assignment.....

S.No.	Date	Topic Covered / Exercise Completed	No. of classes. Remarks
		Unit-I.	
		Introduction to Ic Technology	
		MOSFET Fundamentals	
	1/8/22	Ic fabrication steps	
	to	NMOS fabrication	19
	18/18/22	Pmos fabrication	
		Cmos fabrication	
		Integrated capacitors & Resistors.	
		Unit-II.	
		Basic Electrical properties	
		Nmos Characteristics	
		I_{ds}, V_{ds} Relationships	
		I_{ds} Equation in Linear & Saturation region.	12
	1/9/22	Different Inverter Configurations	
	To	Transconductance	
	15/9/22	o/p Conductance	
		pass Transistor Logic	
		Cmos Inverter analysis and design	
		Bicmos Inverter analysis.	
		Unit-III.	
		mos layers	
		Stick diagram	

LECTURE RECORD

S.No.	Date	Topic Covered / Exercise Completed	Remarks
		Layout Design rules for layout Design procedure for layer	
	16/9/22 to 30/9/22	Design rules for wires and contacts Layout diagrams for NMOS, PMOS and CMOS Design of layout for logic gates Design of layout for AOI & OAI Layout design for combinational circuit.	12 Tutorial 30/9/22
		Unit - IV Sheet Resistance Applying Sheet Resistance to	
	03/10/22 to 25/10/22	MOS Transistor & Inverter gates Standard gate Capacitance and area capacitance Calculation Delay Unit and Inverter Delays Estimation of CMOS Inverter delay. Wiring Capacitance & choice of layers.	13
		Unit - V : Scaling theory Threshold voltage variation	
	26/10/22 to 15/11/22	mobility degradation & velocity saturation Hot carrier effect Output Impedance variation with Drain - Source voltage	Tutorial 30/10/22

LECTURE RECORD

S.No.	Date	Topic Covered / Exercise Completed	Remarks
		MOS device models (level 1, level 2, level 3)	
		BSIM Series	
		Charge & Capacitance modelling	
		Temperature dependence	
		process Corners and analog design in a digital world.	
		Unit-VI	
		Introduction to Low power VLSI	
		Overview of power consumption	
		Dynamic power	
		Short circuit power	
	16/11/22	Leackage power	
	to	Low power design through	
	06/12/22	voltage scaling	18
		VTCMOS circuits	
		MTCMOS circuits	
		pipelining & parellel processing	
		Estimation and optimation of Switching activity	
		Concept and Reduction of Switching activity	
		Glitch Reduction	
		Gated Clock Signal.	

6/12/22

21/01/19

UNIT - I

INTRODUCTION

VLSI: Very Large Scale Integration

It is one of the IC Generation, divided based on the No. of components presented in an Integrated Circuit or a chip.

→ There are different classifications of IC Generations

		Components	Example
1.	SSI - Small Scale Integration	1 - 10	Logic Gates (NAND, NOR etc)
2.	MSI - Medium Scale Integration	10 - 100	Adders, MUX, Decoders
3.	LSI - Large Scale Integration	100 - 1000	Sub Systems like ALU, CU
4.	VLSI - Very Large Scale Integration	1000 - 10,000	Systems like 8-bit, 16 bit processors.
5.	ULSI - Ultra Large Scale Integration	> 10,000	Spl processors like CISC, RISC
6.	GSI - Gaint Scale Integration	- billions of transistors	Micro processors Micro Controllers

Introduction to IC Technology:

Discrete Circuit: Consists of discrete components. It is an Electronic circuit which is made with discrete.

26/06/19

Integrated Circuit: It is an electronic ckt which performs the same function as discrete circuit, only the difference is here (in IC's), we can connect more no. of components (millions of components), like Resistors, Capacitors like discrete components in a single small silicon plate (Substrate)

Need of IC's:

1. Small in Size - Portable
2. Low cost because they are produced in large no.
3. Speed is high because the transition delays in IC's are very less since the components are small compared to discrete components.
4. Reliability - Highly reliable
5. Power consumption is low bcz of its small size thereby heat Generated is less.

improved performance

ICs may be Linear or Digital

Technologies:

* Based on the components' used, IC Technologies are

BJT Technology

Nmos "

Cmos "

GaAs "

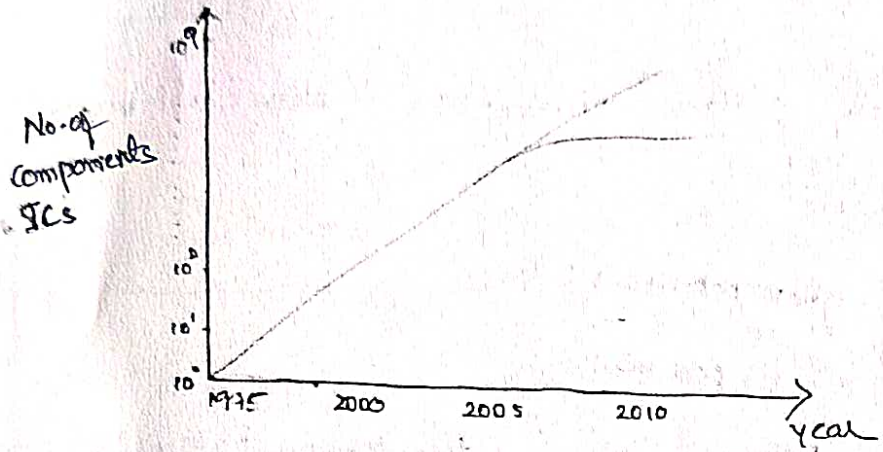
MOSFET Technology

In MOSFET's, the channels acts as conducting paths for the flow of e's from Source to drain & this channel length describes Technology. Ex: 22 nm Technology means channel length is 22 nm.

6. Based on the size of components, Jordan Moore, an Industrialist implemented a law in 1960's ✗

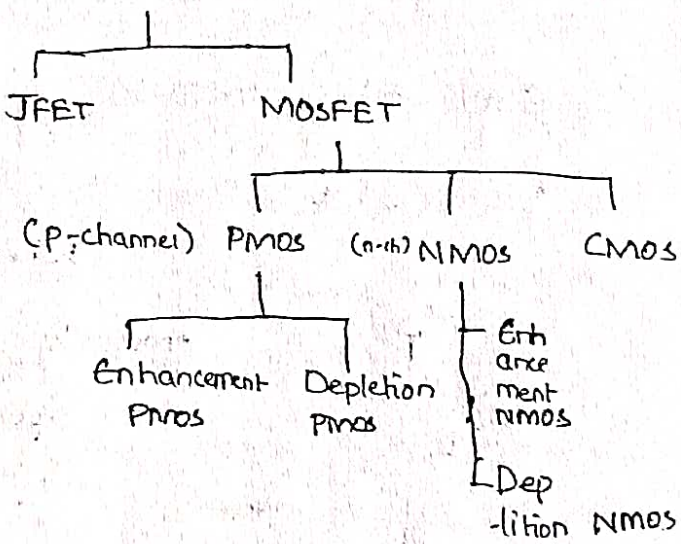
→ In 1960's, Gordon Moore proposed Moore's law related to no. of components present in a IC's

Moore's law: Moore's law states that the no. of components presented in the IC would grow exponentially and it doubles for every 18 months (1½ year)



27/06/18

MOSFET Fundamentals:



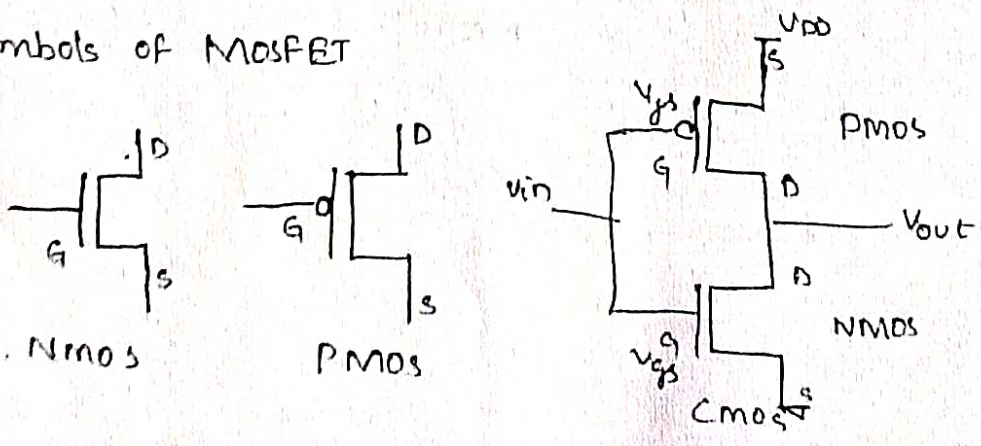
CMOS: Combination of PMOS & NMOS

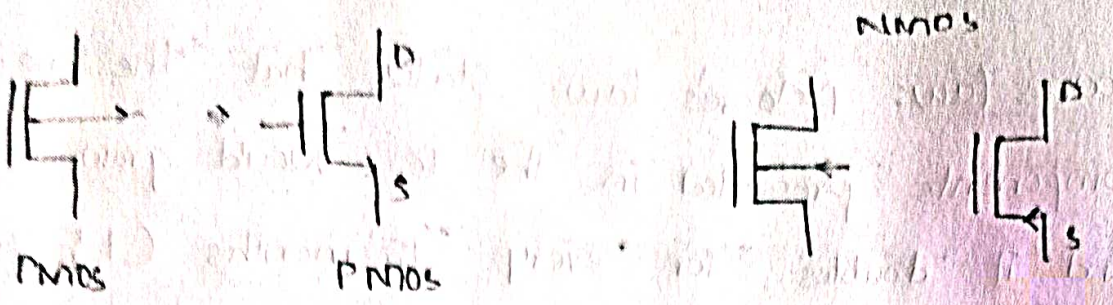
Enhancement MOSFET:

Here, the channel is enhanced by applying external gate potential b/w the source & drain

In Depletion MOSFET, the channel is implanted during fabrication b/w source & drain terminals

Symbols of MOSFET





* Bulk terminal is to control threshold voltage of device

$V_t = 0.2 V_{DD}$

PMOS Source — higher potential

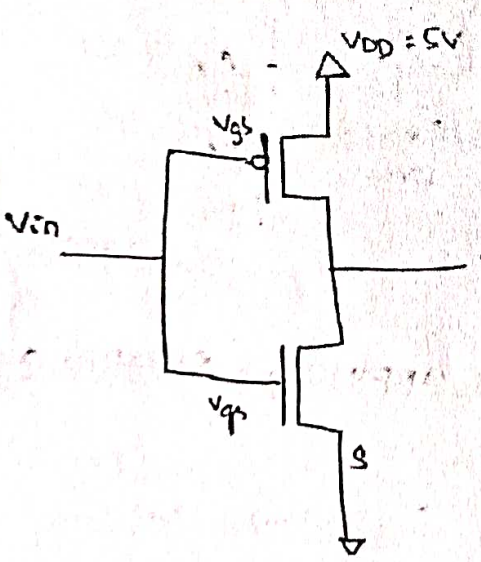
NMOS Source — lower potential.

Gate voltage of PMOS is -ve ⟨to attract holes & form Channel⟩

Gate voltage of NMOS is +ve ⟨to attract e^- & form Channel⟩

Gate voltage must be greater than Threshold voltage.

$V_{gs} = V_g - V_s$



When $V_{in} = 0$ V

PMOS: $V_{gs} = V_g - V_s = 0 - 5 = -5V$

NMOS: $V_{gs} = V_g - V_s = 0 - 0 = 0V$

∴ PMOS is ON

output is 5V

When $V_{in} = 5$ V

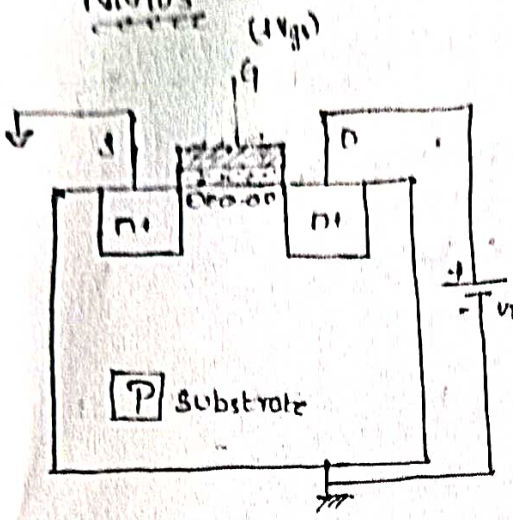
PMOS: $V_{gs} = V_g - V_s = 5 - 5 = 0$

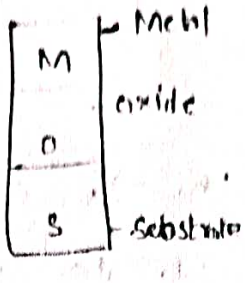
NMOS: $V_{gs} = V_g - V_s = 5 - 0 = 5V$

∴ NMOS is ON & o/p is 0V

28/06/18 Characteristics

NMOS





Threshold Voltage V_t:

It is the voltage at which the device conduction starts.

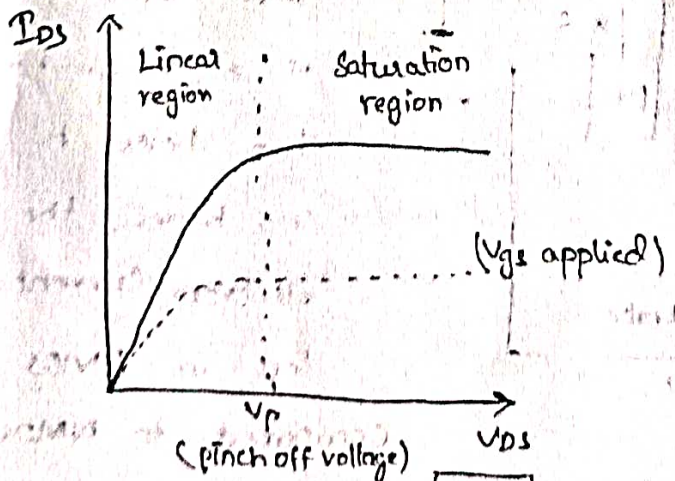
→ The channel is called Inversion layer.

Effective Gate voltage: $(V_{gs} - V_t)$ The Gate voltage at which the channel is formed.

* Before applying the V_{gs}, channel is weak inversion layer
* When $V_{gs} > V_t$, channel is strong inversion layer.
* Current is controlled by the Gate Voltage & V_{DS}.

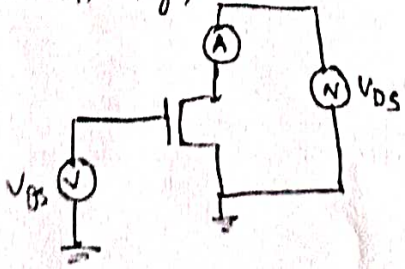
→ If width of channel is more, more current is obtained

Since V_{DS} is given at Drain; e^- move from Source to Drain & the current flows flows from D to S



* When V_{DS} is continuously increased, pinch off occurs at particular voltage & the current would be constant (saturated)

CKT dig:



Note:

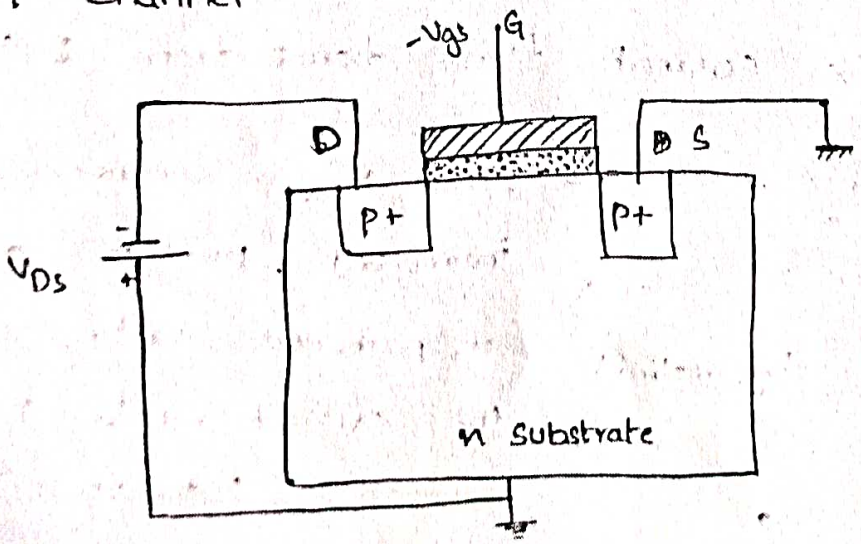
- To establish Channel: $V_{gs} > V_t$ [Effective Gate Voltage]
- Linear region / Non Saturation region: $(V_{gs} - V_t) > V_{ds}$
- Saturation Region: $(V_{gs} - V_t) \leq V_{ds}$
- In linear region, MOSFET can be used as a Resistor.
- MOSFET can also be used as a Switch.
- Channel Modulation: Due to variation in V_{DS}, Chanel length varies

  When V_{DS} ↑, channel length ↓ (due to depletion region increment)

  i.e., e^- in the channel gets attracted to +ve voltage (V_{ds})

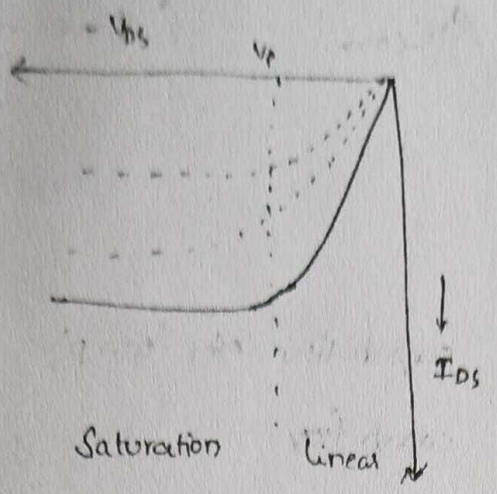
PMOS:

P Channel MOSFET:



V_{DD}

Since mobility of e^- is greater than holes by 2.5 times, the electron current is less in PMOS compared to NMOS.



As V_{gs} ↓, current also decreases.

$|V_{gs}| < |V_t|$ — cutoff

$|V_{gs}| \geq |V_t|$ } linear

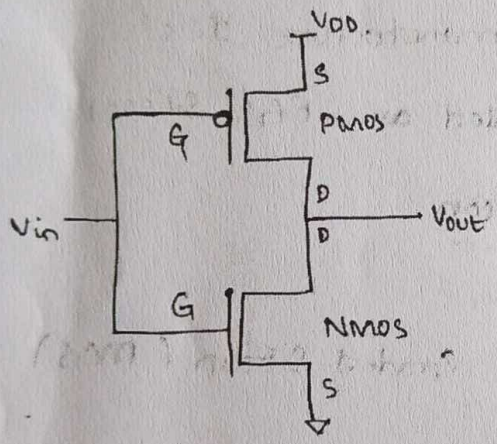
$|V_{ds}| < |V_{gs}| - |V_t|$ }

$|V_{ds}| \geq (|V_{gs}| - |V_t|)$ — Saturation.

28/06/18

CMOS : Complementary MOSFET

→ Combination of PMOS and NMOS



In designing, the terminals Source & Drain are Interchange - able.

IC fabrication Steps:

1. Crystal preparation
2. Wafer preparation
3. Epitaxial Growth
4. Oxidation process
5. Photo lithography Technique
6. Etching process.
7. Diffusion "
8. Metalisation
9. Packaging
10. Testing

* Material Required: Silicon (Semiconductor)

Advantages of Silicon:

1. Availability
2. Resistivity (Withstanding capability of temp)
3. Temperature withstanding capability
4. Electron Band Gap
5. Mobility (GaAs has more mobility but its compound Semiconductor & costly)

* Pure Silicon is required to manufacture IC's
(99.9999 % pure silicon - called as EGS - Silicon)
EGS - Electronic Graded Silicon.

* Raw material : SiO_2

* 98% pure Silicon : Metallurgical Graded Silicon (MGS)

* EGS is available in liquid form

* Crystal Preparation:

Single Crystal Silicon - From this we obtain Substrate (Silicon plate)

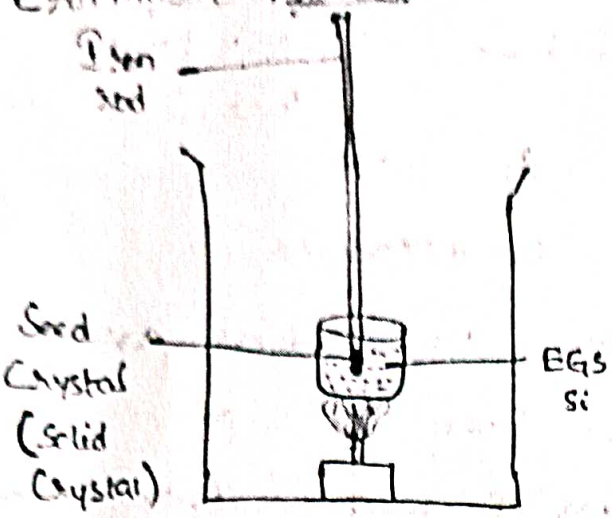
* Substrate is a silicon plate on which we are making the physical circuit. Substrate is obtained from the Single Crystal Silicon. Single Crystal Silicon is a solid form of Silicon made from Electronic Graded Silicon (EGS) (liquid)

Mostly used methods are:

① Bridgeman method

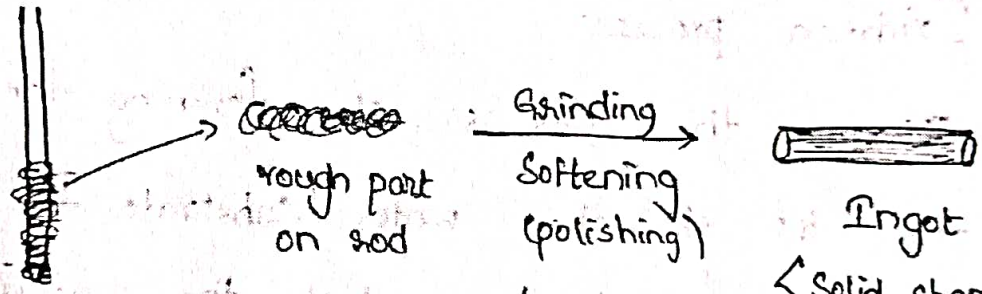
② Czochralski method.

Czochralski process.



* First heat EGS around 1000 - 1200°C
* Dip the seed crystal into EGS with the help of iron rod.
3. Pull out the iron rod by rotating from the bowl

* After cutting the rough part formed on the rod, it is sent for grinding process & Softened.



* length of Ingot would be of 1 to 2 metres
* Diameter : 75mm - 250mm & bears 60kgs of EGS
* After slicing the ingot ( ) we get disc shaped plates which is called wafer ( )

Wafer preparation:

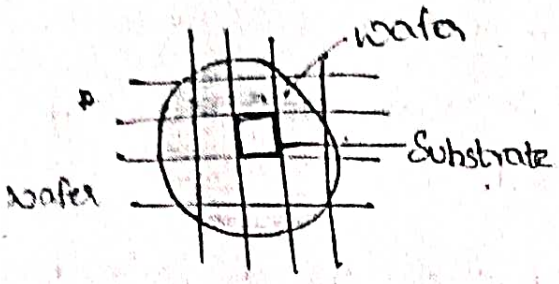
Wafer is a disc shaped Silicon plate obtained by slicing the Silicon Ingot. (Slicing process)

→ Diameter : 75mm - 250mm - 1 to 30 cm
→ Thickness : 250μm - 400μm 1 to 600 μm

* Wafer

5. Epitaxial Growth: No. of Silicon layers added to improve thickness of layer

Epitaxial is a Greek word: Epi : upon
taxial : ordered



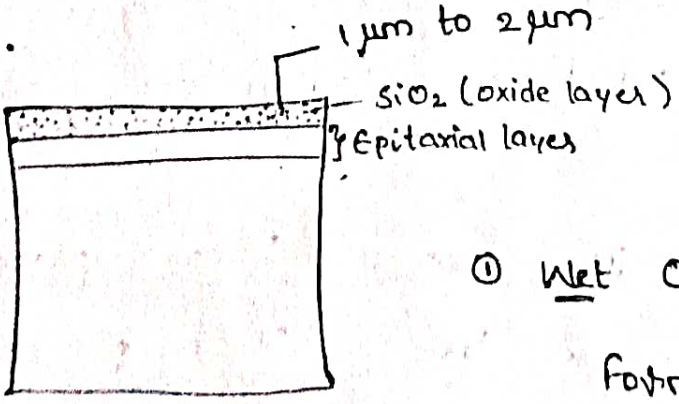
Not only Silicon layers, adding isolation layers to improve thickness of wafer is Epitaxial Growth

< only upto little level because, characteristics may change if many layers are added.

4. Oxidation process:

It is the process of forming the oxide layers on the top of the wafer / substrate. It is a insulation layer used to protect the wafers & fabricating devices from the external impurities & environment.

6. ~~Photo Lithography Technique~~



① Wet Oxidation:

Formation of oxide layer using water at high temperature

$Si + 2H_2O \longrightarrow SiO_2 + 2H_2$

(Oxide layer)

CVD

→ Chemical Vapour Deposition

Oxidation:

$Si + O_2 \longrightarrow SiO_2$

(Oxide layer)

* Diffusion process: Adding impurities like p-type dopands and n-type dopands.

Lithography: producing required patters (like mask)

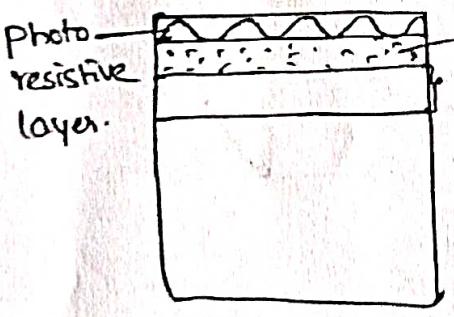
5: Photo Lithography: Technique used to produce required patterns using ~~res~~ photo resistive layers & UV rays.

Photo resistive layers: 1. Positive Resistive layer

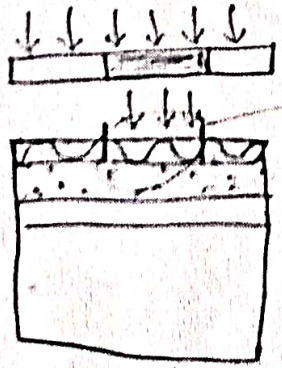
2. Negative " " "

chemical.

This Resistive layer is placed on the oxide layer. (Chemical)



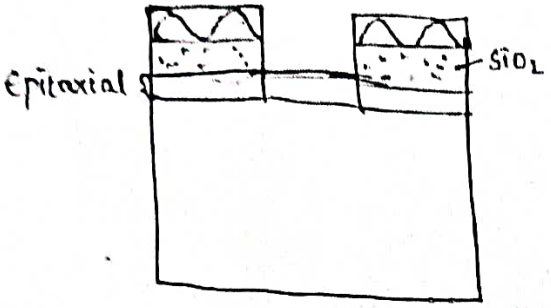
To make a well on the resistive layer we use a layer. The part where the well is to be made is placed below the chromium layer and the UV rays are passed.



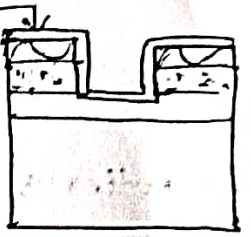
Chromium layer allows UV rays. Then that portion beneath becomes soft. < for positive resistive layer)

* For -'ve resistive layer, the portion allowed by the UV rays becomes hard <opposite to +'ve layer>

6. Etching: Removing the unwanted material or unwanted portion on Substrate. It is used to add the dopands on removed portion for making the devices.

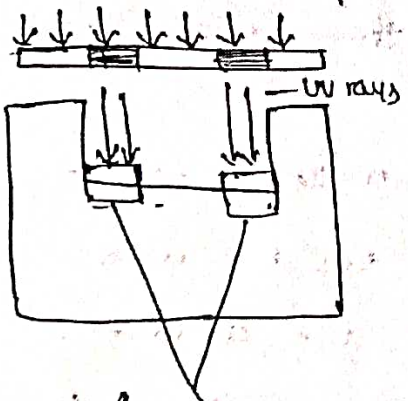


Now, to protect this a thin oxide layer (< 1μm) is coated around the well. before adding impurities.



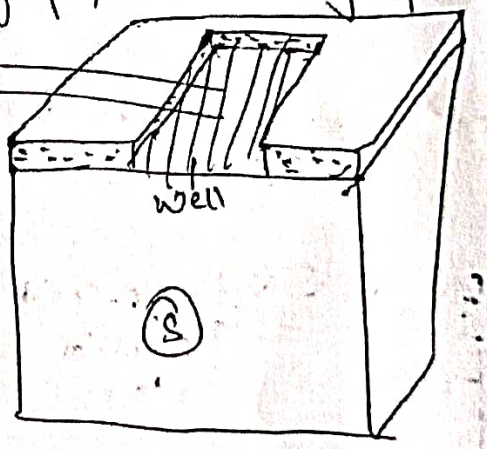
7. Diffusion: Process of adding dopands on required portion in a Substrate.

Again, here we use Lithography & etching process to add dopands.



Softens & Can be removed for doping

Doping:

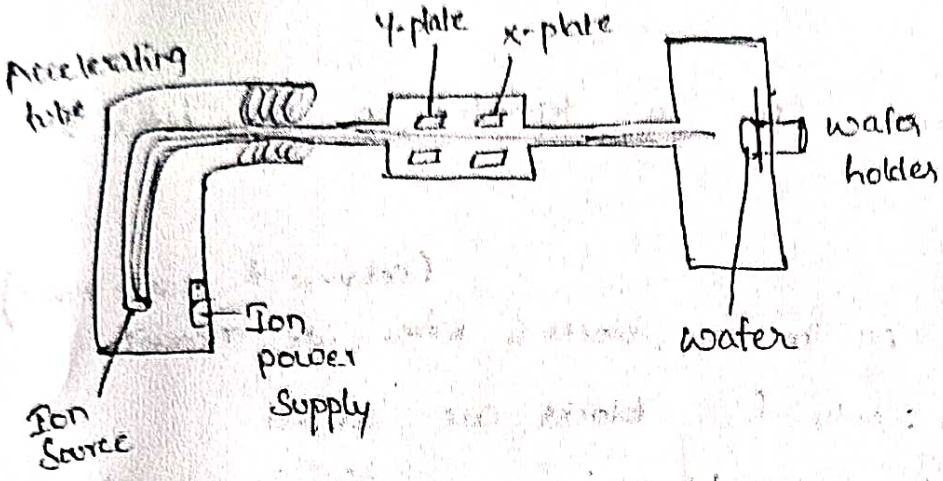


Dopands: P-type : Boron
n-type : Arsenic, Phosporous

Etching is of 2 types:

1. Wet etching : using chemicals. fast process.
2. Dry etching or Plasma Etching : Sputtering process. takes much time but high / better Electrical properties

Ion implantation : Method used to diffuse the dopants into the wall using Ion source to form Source & Drain terminals

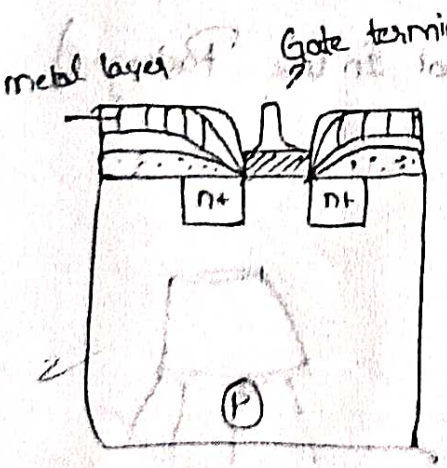


From the ion source, the dopants get move ~~to~~ along the accelerating tube through the plates and settle on the wafer at required position

02/07/18

8. Metalisation : It is the process of depositing the Metal layer over the surface of the Substrate / wafer.

- Provides the metal layers of interconnecting wires for connecting the components in a (chip) Integrated Circuit. This can be done using CVD process at 1000° to 1200° (CVD - Chemical Vapour Deposition).



- The chip is tested before packing. To check if any bad chips (with faults) are present.
- Physical testing is conducted before packing to check all the components are

9. Packing Packaging: Encapsulation & sealing the circuit in a case is Packaging with Glass enclosed cover case.

* Initially Organic Epoxy is deposited in tiny blocks in IC

(Ceramic & plastic case)

1. Fully closed : All the tiny blocks & wires are encased.
2. partially closed : only few blocks are sealed
3. Open : If single block is present, it is opened.

Sir → * This is the final stage of fabrication process of IC. In this, the tiny blocks of Integrated ckts are encapsulated with a glass type material (depositing the Organic Epoxy) to protect from the physical damage and corrosion.

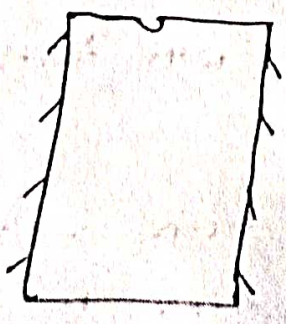
Encapsulation : Protecting ckt for corrosion

→ done in 3 ways : Fully closed, partially closed, Open.

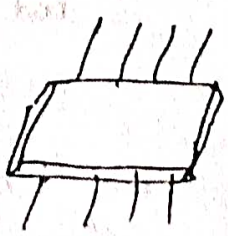
packaging can be done for multi chips also & for only single chip.

Mostly used packaging is DIP (Dual In line Package)

Types of packing:



DIP



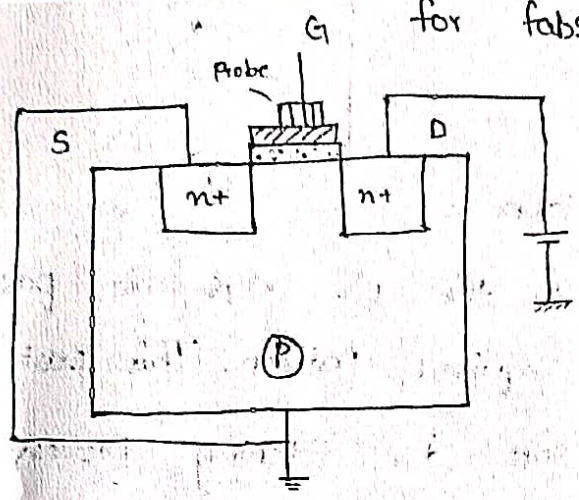
Flat pack

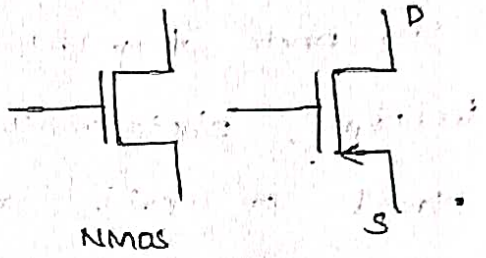
Metal can

Testing: Verifying IC by checking the functionality.

→ Equipment for testing IC's - IC Testers.

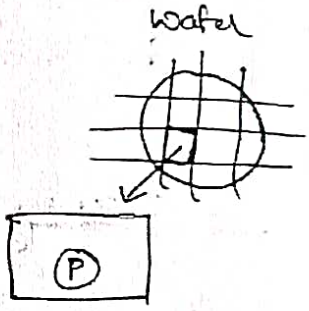
NMOS Fabrication: Structure of the device is to be known for fabrication.





Preparing P-type Substrate:

① P-Substrate is obtained from Si Ingot



P-type Ingot $\xrightarrow{\text{Sliced}}$ wafer $\longrightarrow$ P-Substate.

P-type Substrate is obtained from Si Ingot by adding P-type dopands (Boron) in the Substrate.

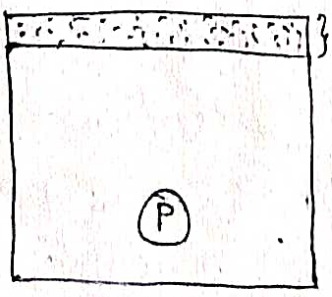
② Epitaxial Growth : It is optional.

optional

* If thickness is satisfactory, no need to add any Si layers to wafer. Adding Si layers also changes its characteristics.

③ Formation of Oxide Layer: (Oxidation)

→ To protect the wafer from external Impurities.



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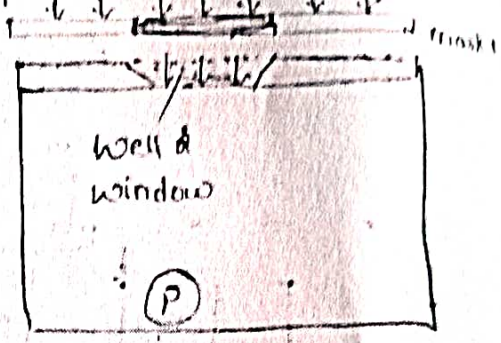
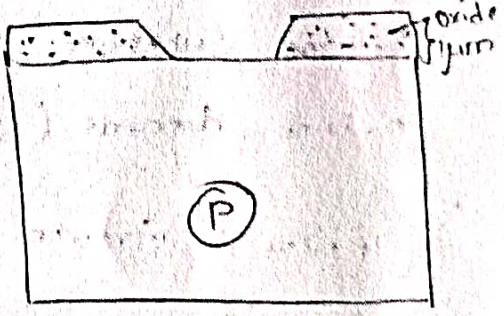
(3). Photo Lithography Technique: Photo resistive layer is placed upon the oxide layer to prepare a well.

→ Create a well on oxide layer
window

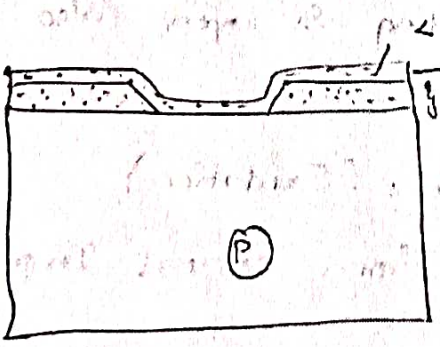


* Using photo lithography technique, photo resistive layer is placed on oxide layer & the UV rays are passed through the layer in required pattern. This part can be removed & made soft by Etching process.

→ Etching: Using Etching, we remove the soft portion on the resistive layer to form Source, Drain & Gate terminals.

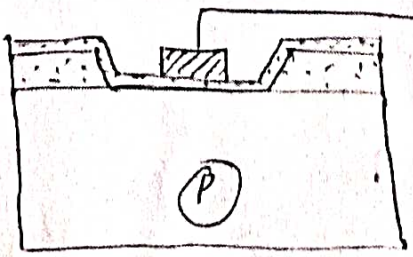


→ After Etching process, formation of thin oxide layer to form the ~~ext~~ MOSFET Structure



< Using CVD Chemical Vapour Deposition oxide layer is formed.

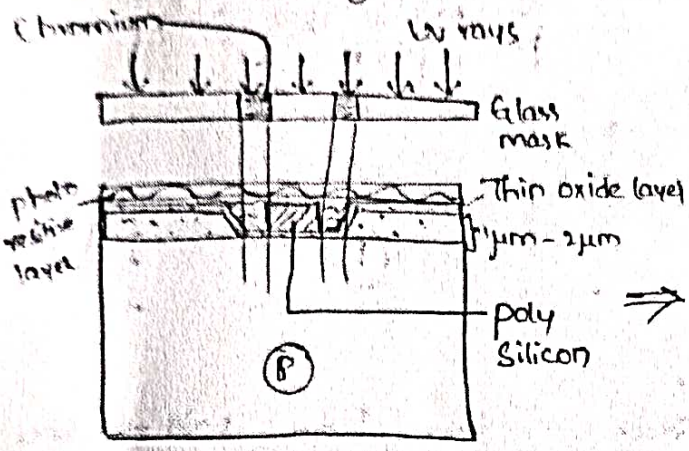
Depositing pattern poly Silicon: On top of thin oxide layer for Gate terminal.

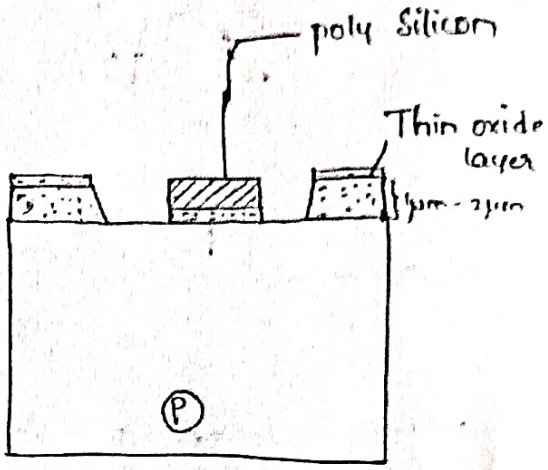


< placed through CVD >

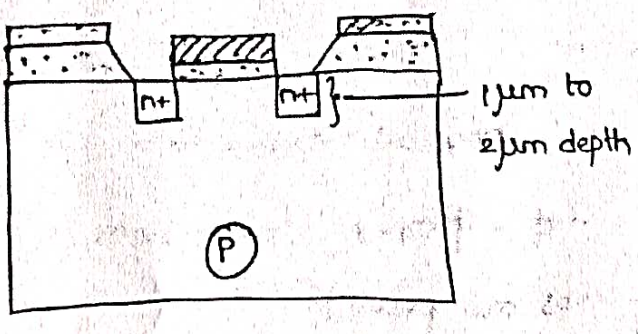
Diffusion: Introducing impurity in required portion of Substrate to form the Source & Drain terminals. This process is called Diffusion process.

* Photo. Lithography & Etching are again performed.



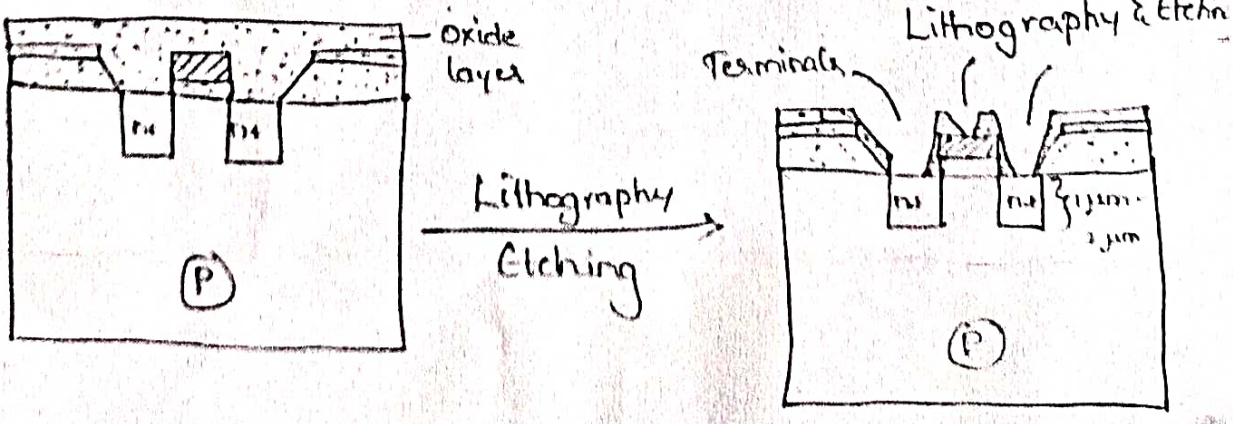


Ion Implantation: To diffuse ions (n-type ions: Arsenic, Phosphorous)

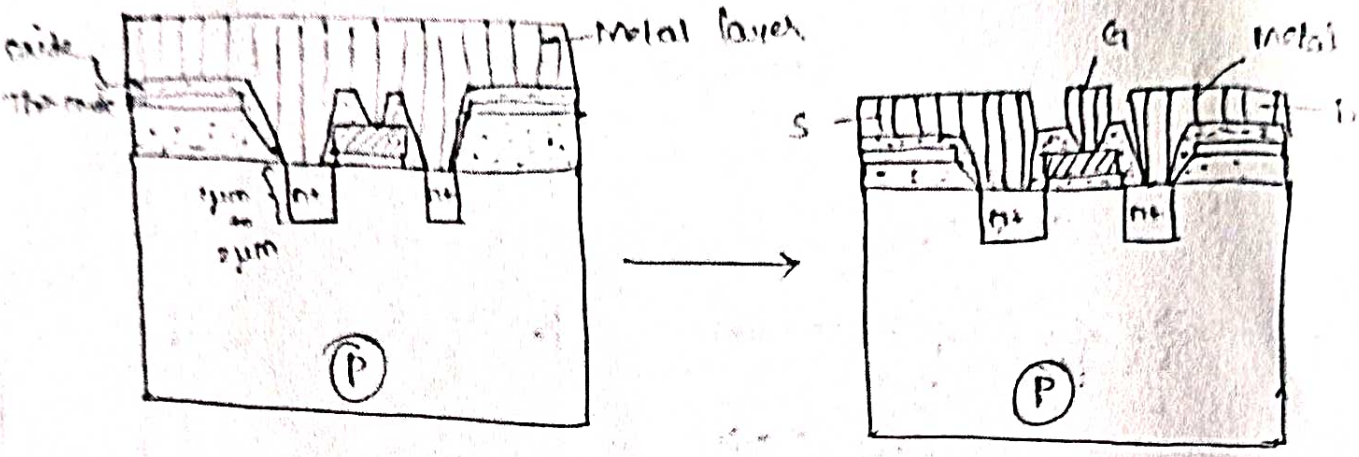


Metalisation: Before Metalisation, Contact cuts are to be done

Contact cuts (contact holes): First another Oxide layer (Insulating layer) is placed over the device & later 3 contact cuts are made for 3 terminals (Gate, Source, Drain) using



Metalisation: Depositing the metal layers on top of the oxide layers. (Metal used is Al, Copper)



Mostly copper is used since it has high withstanding capabilities.

Testing: Checking whether all the layers are present & not and then encapsulating

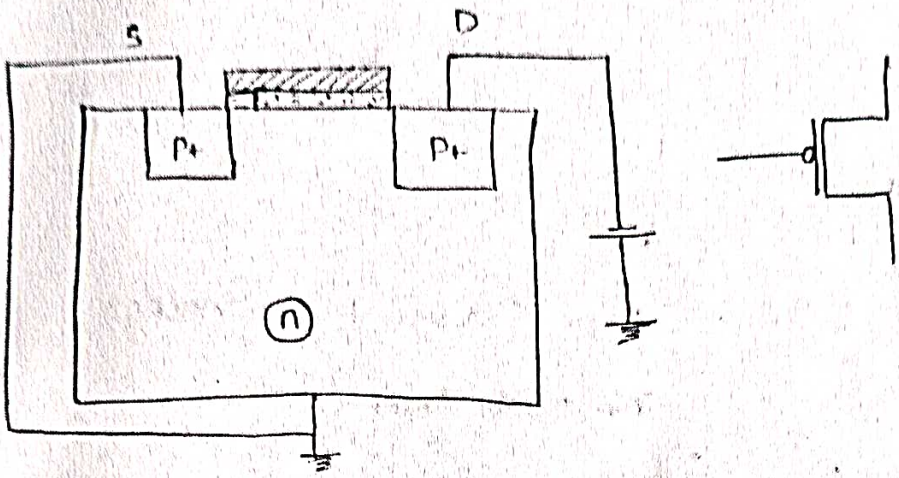
* Physical Testing: Checking physical connections of devices for proper placing and proper connections (Short ckts (if any overlaps are present)

and Encapsulation: Seal the individual parts in IC by depositing Epoxy

PMOS Fabrication:

Doping concentration:

1. Structure of PMOS:

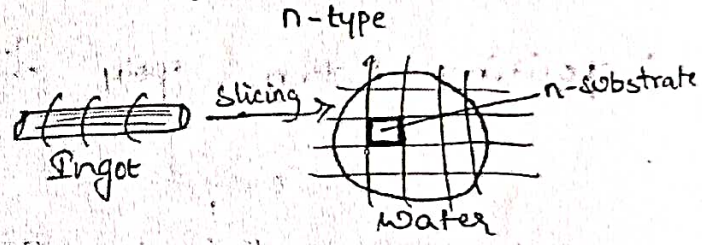


n - Substrate is obtained from the Silicon Ingot

n-type Ingot $\xrightarrow{\text{Sliced}}$ wafer $\longrightarrow$ n substrate.

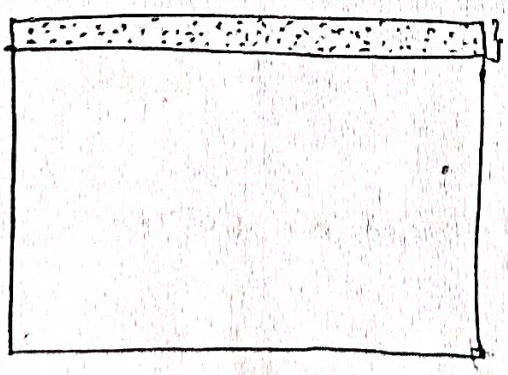
n-type is obtained from adding the v dopands (P, As) in the Substrate.

Epitoxial Growth: optional

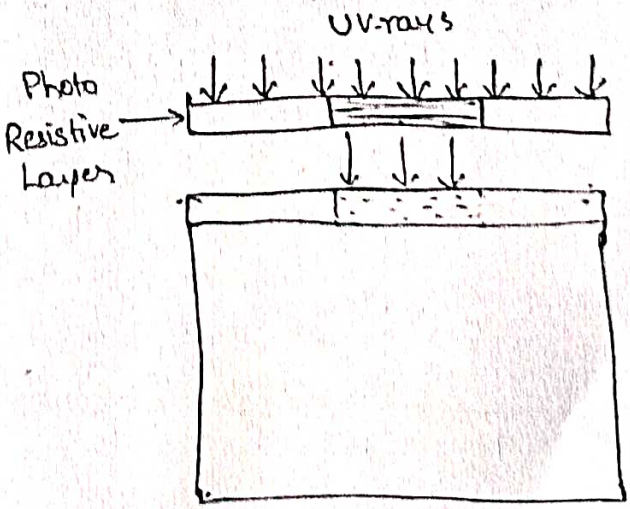


2. Formation of Oxide layer:

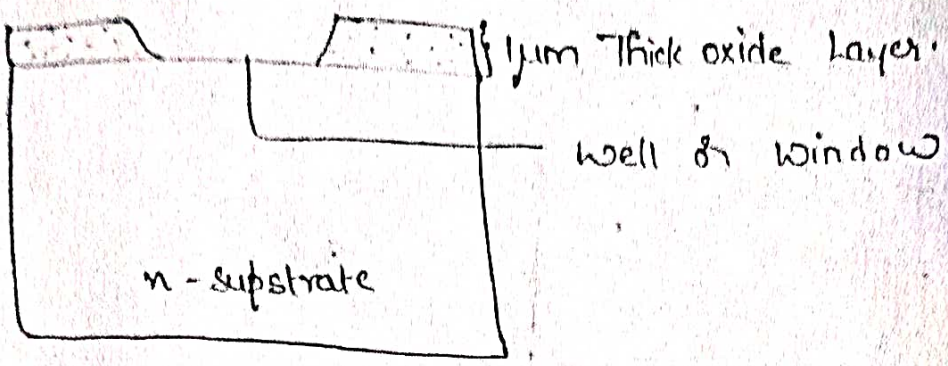
To protect wafer from external impurities.



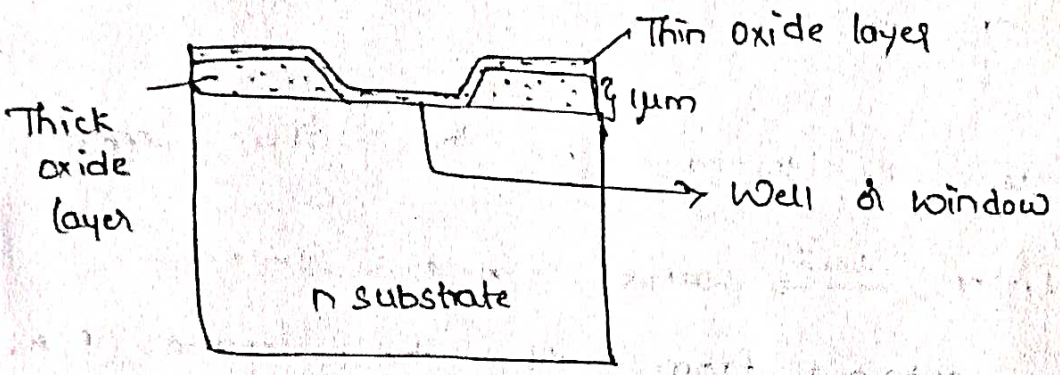
3. Photo Lithography:



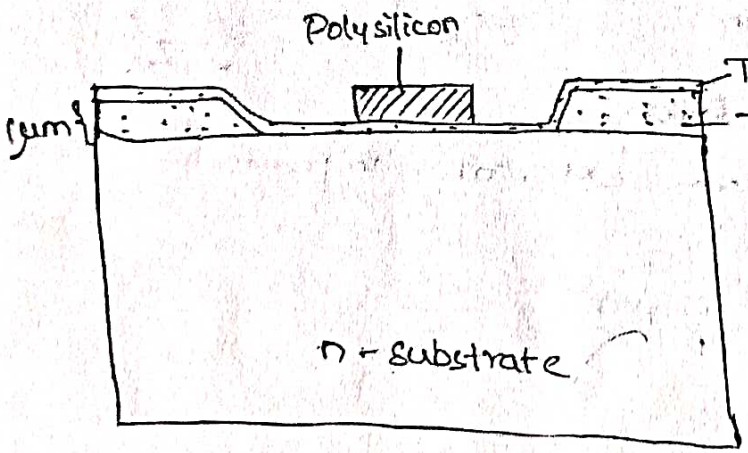
Etching: Softened part is removed.



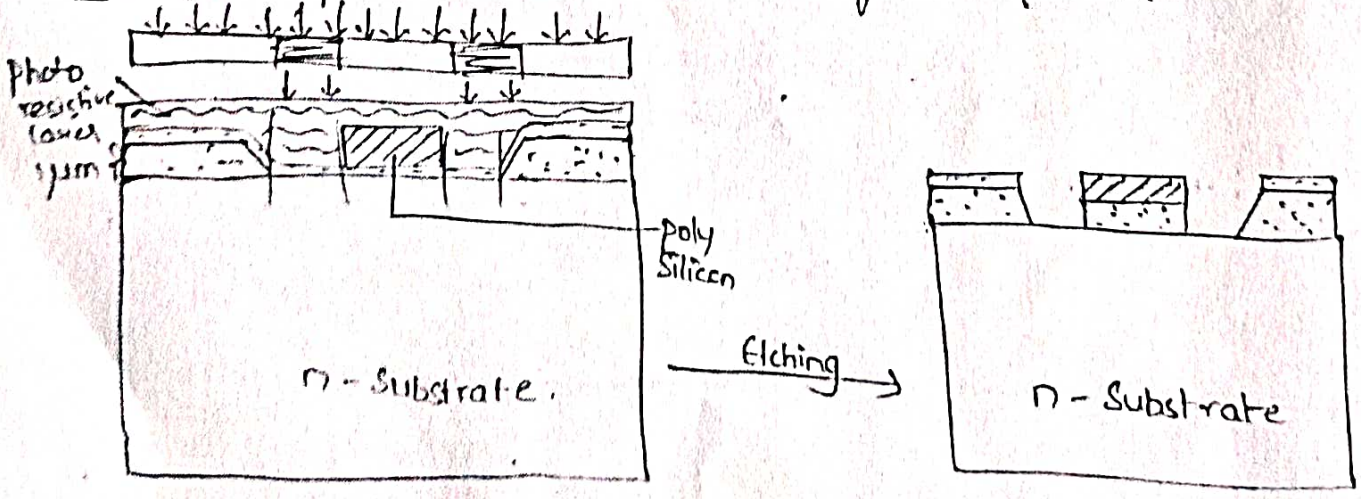
After etching, oxide layer is placed over the MOSFET



Depositing pattern poly Silicon : For the sake of Gate Terminal through CVD proce



Diffusion: Dopands are added at required pattern.

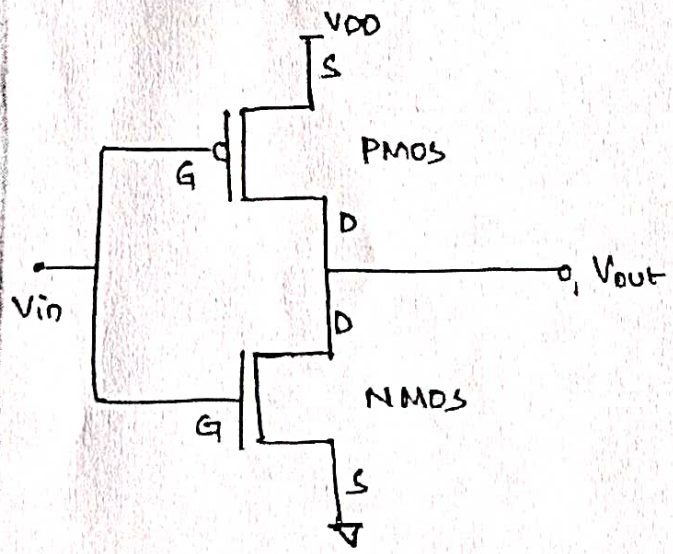


04/07/18

CMOS Fabrication:

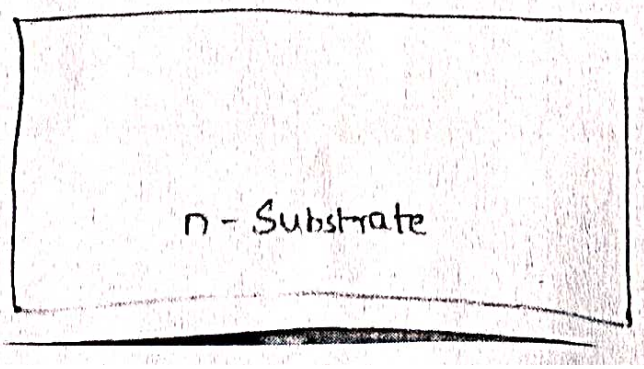
- CMOS can be fabricated in 4 ways:
  1. P - well process
  2. N - well process
  3. twin - tub
  4. SOI - (Silicon on Insulator)

*. CMOS Circuit:

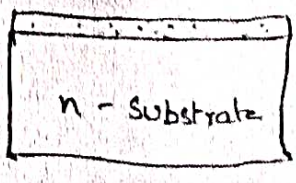


1. Fabrication of CMOS using P- Well Process:

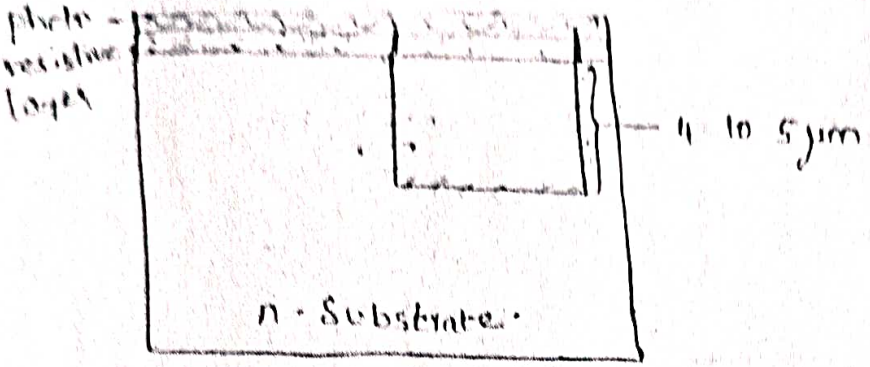
1. Prepare the n-type Substrate : By adding n-type dopands.



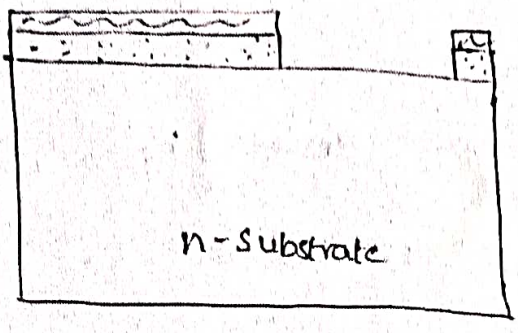
2. Formation of oxide layer on substrate



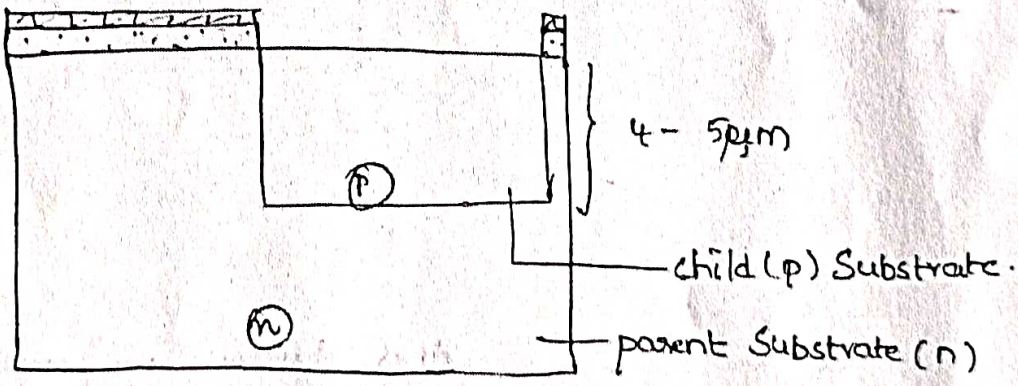
3. Create a p well in n-Substrate using Lithography technique



After etching, p-well

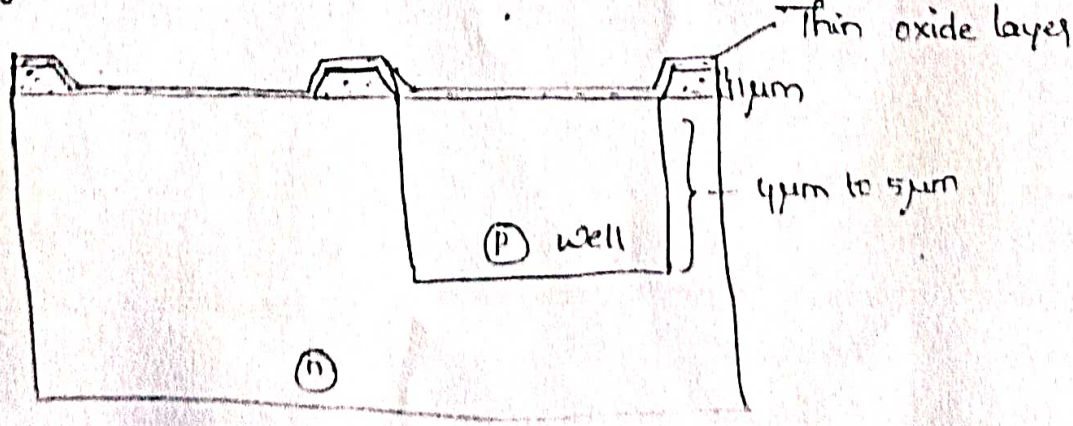


Now, diffusing the p type ions into the substrate.

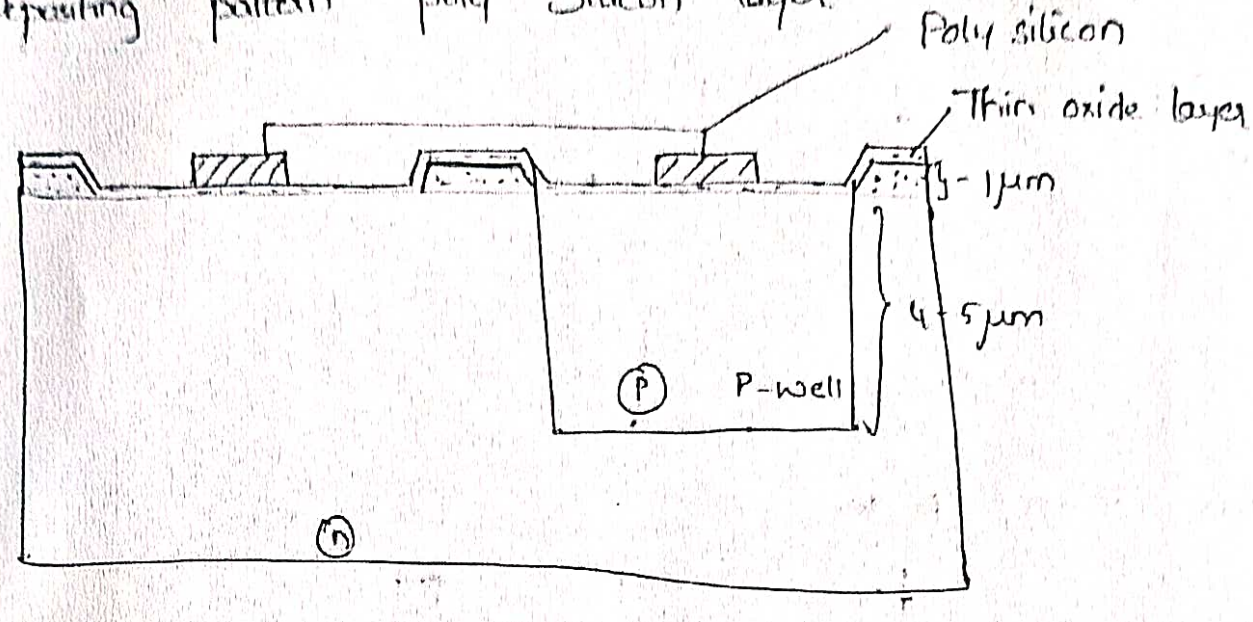


Now depositing thin oxide layer & applying poly silicon for Gate terminal.

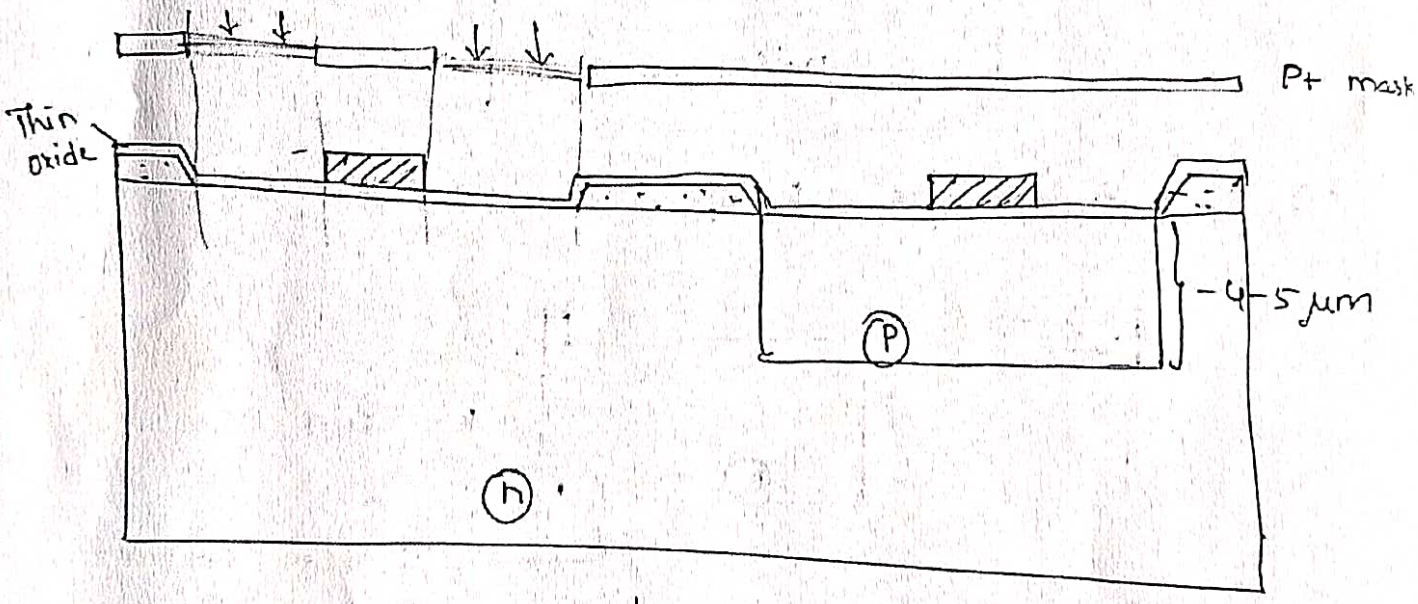
→ On the other side; another oxide window is to be formed through Lithography & Etching.



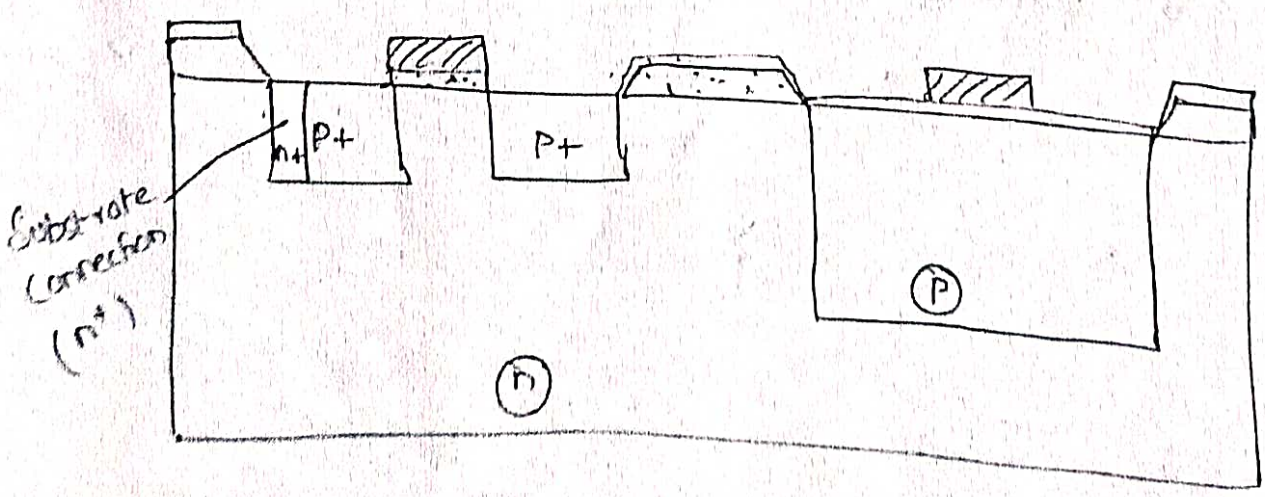
Depositing pattern poly Silicon layer.



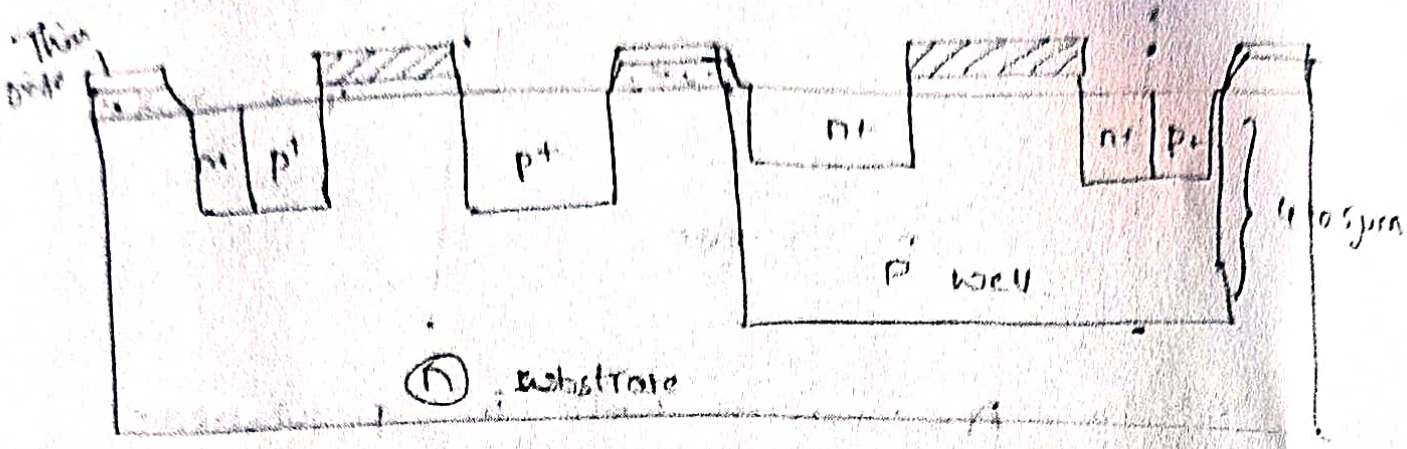
* Fabricating P-MOS device by P^+ diffusion



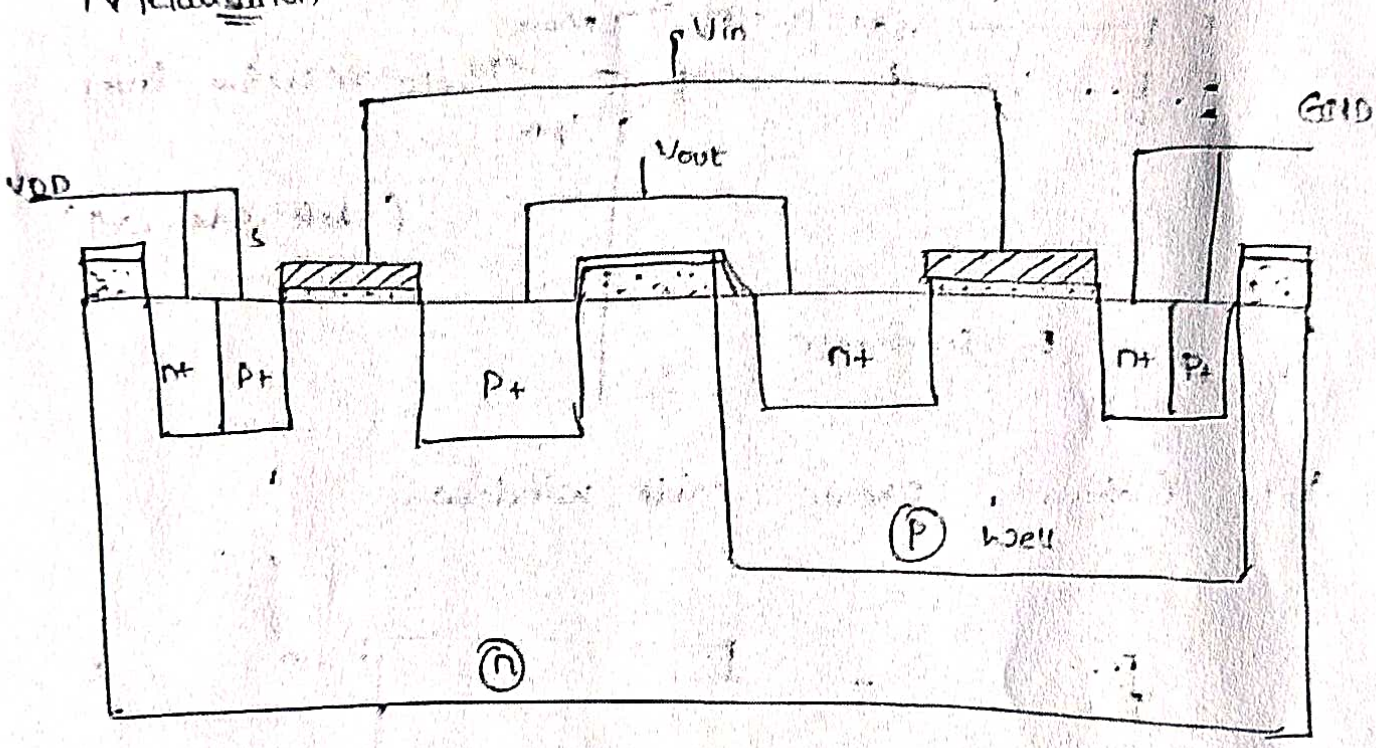
After diffusing P+ ions



Fabricating N-MOS by diffusing n+ ions in p-well.

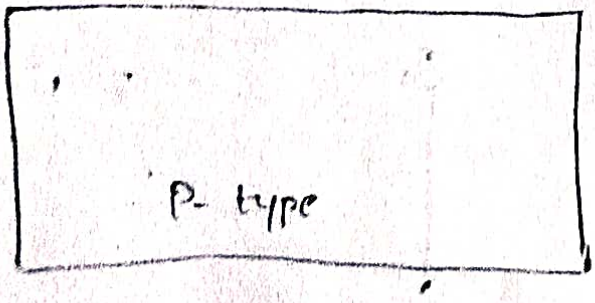


Metalisation

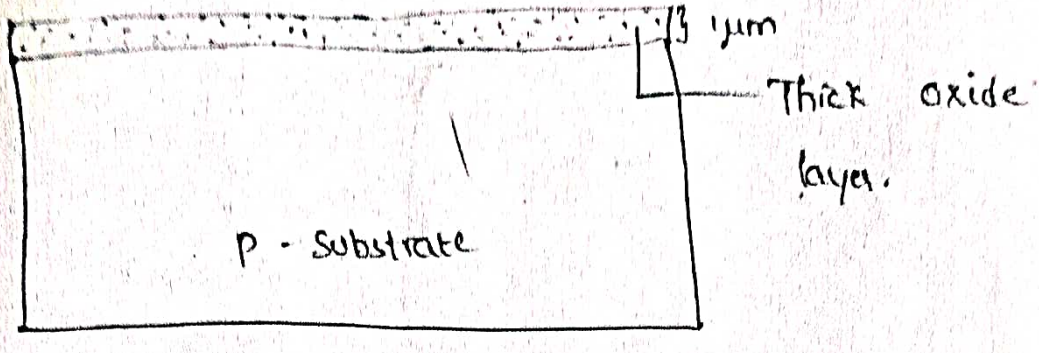


⇒ N-Well Process:

1. Prepare p-type substrate: By adding p-type dopands

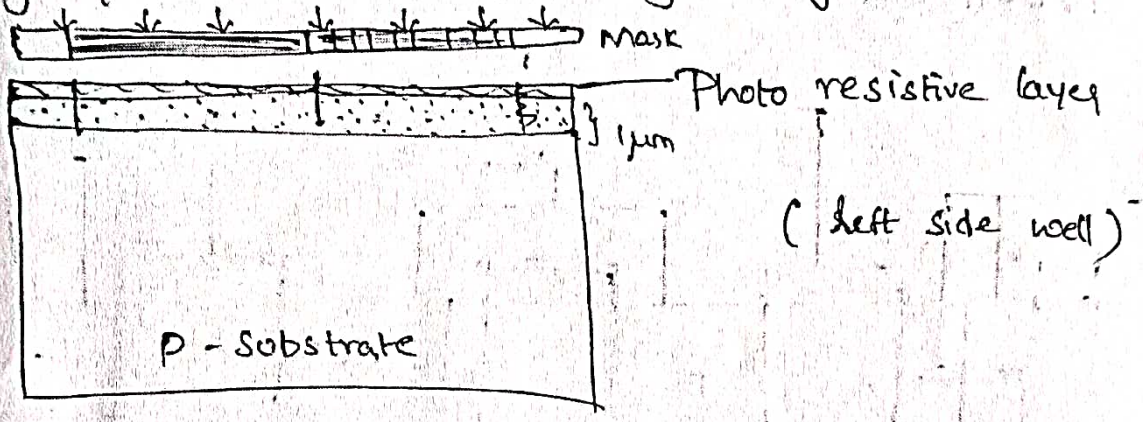


2. Formation of oxide layers on Substrate:

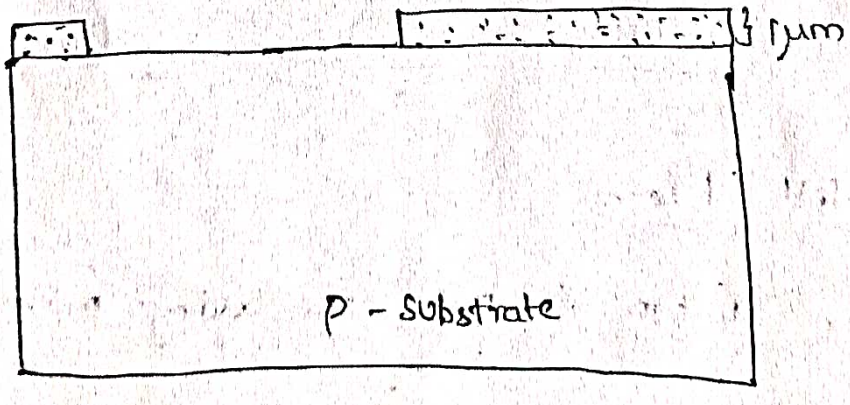


3. Create a N - substrate well in p substrate.

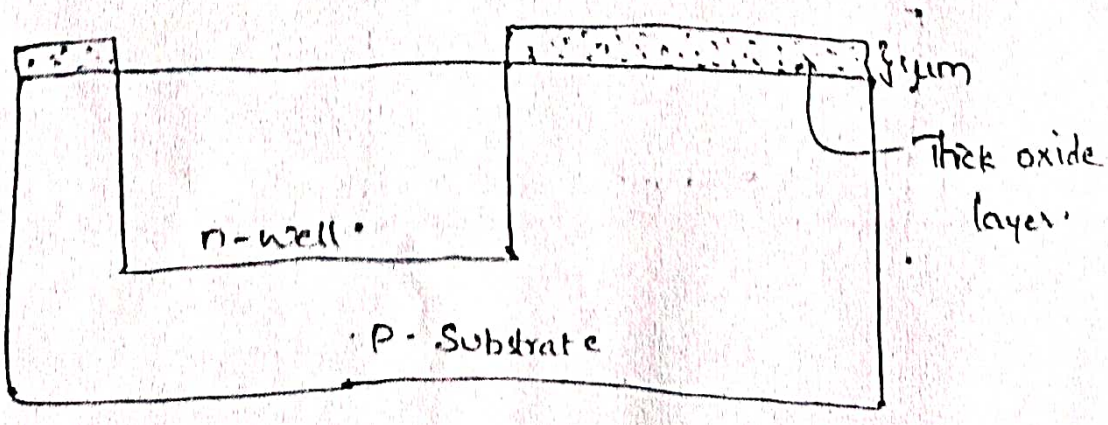
Placing photo resistive layers using Lithography.



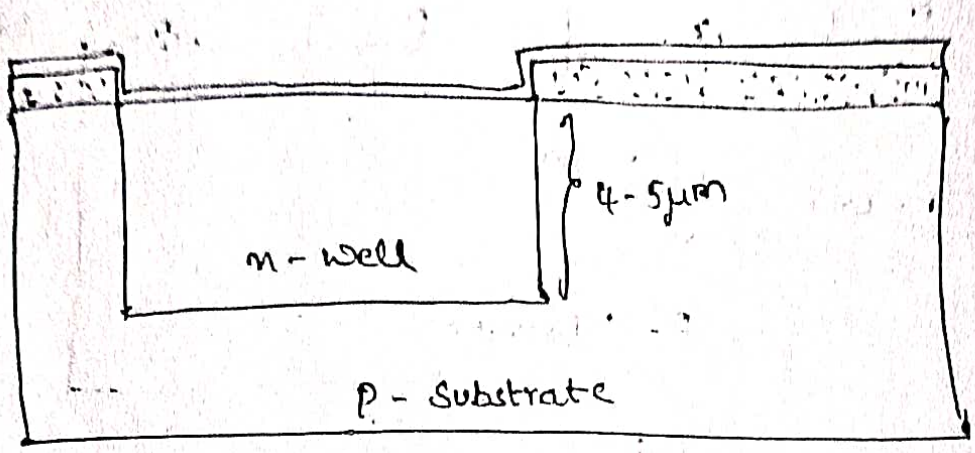
After Etching, create oxide window.



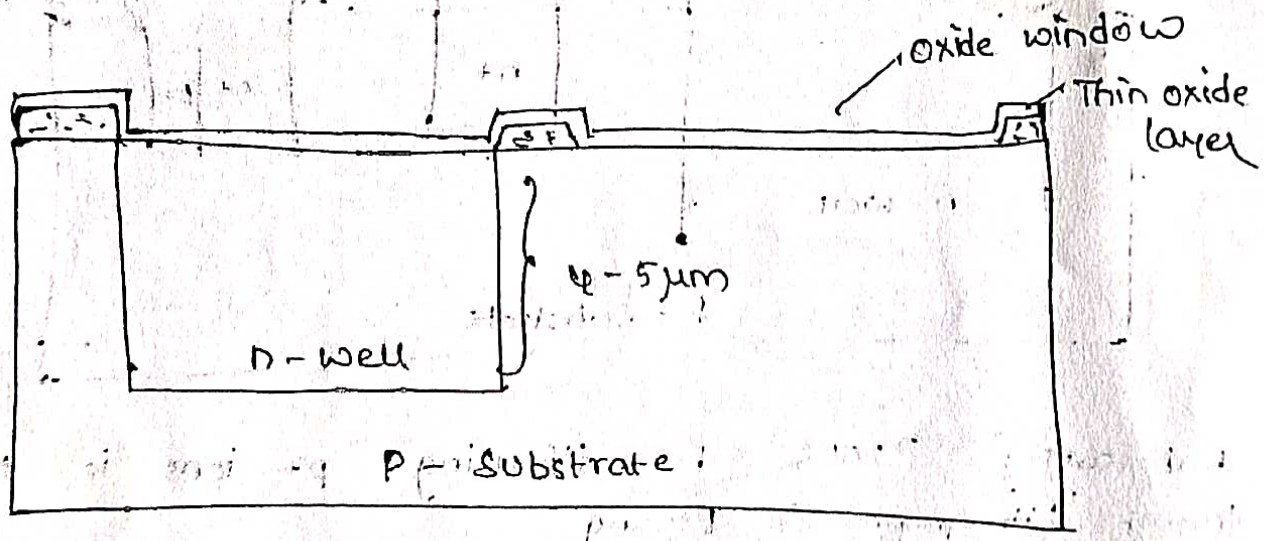
Now diffusing n - type ions in p - substrate



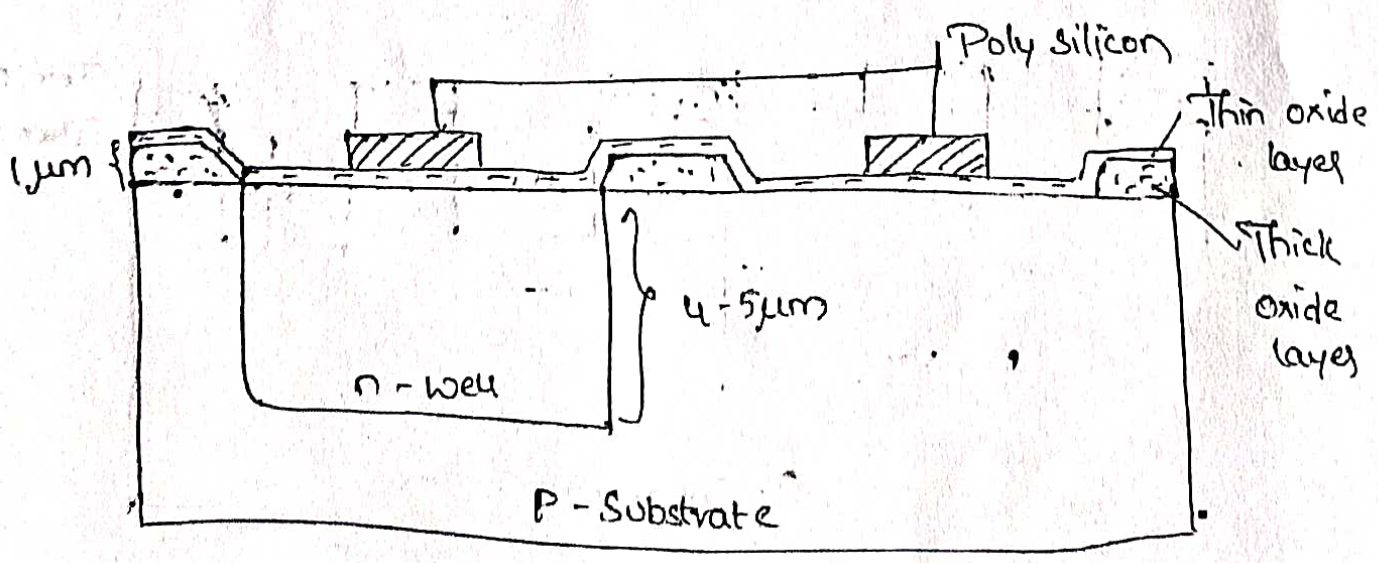
Depositing thin oxide layer on the device.



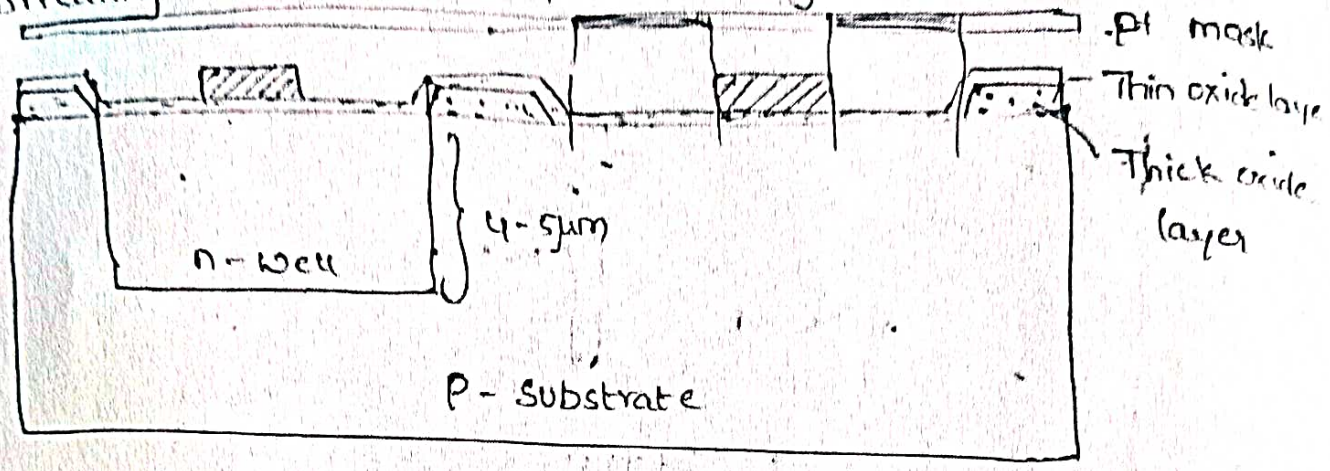
Now Creating another oxide window through Lithography and Etching, we get



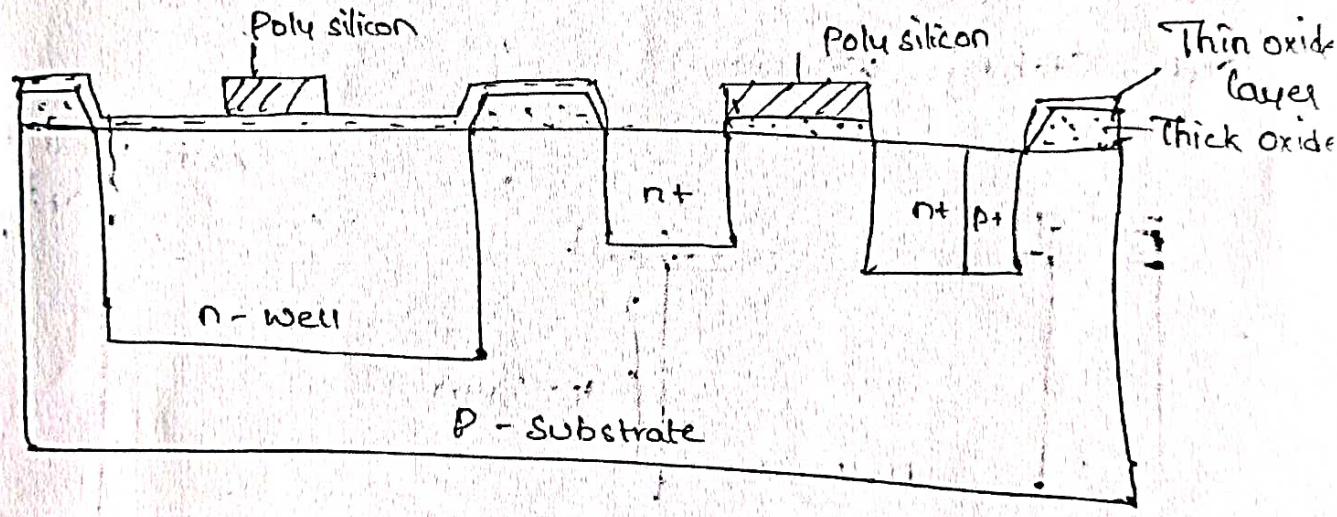
* Depositing pattern poly silicon to form Gate



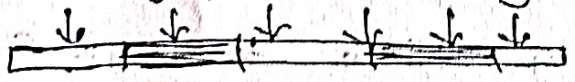
Fabricating N-MOS by diffusing n+ ions

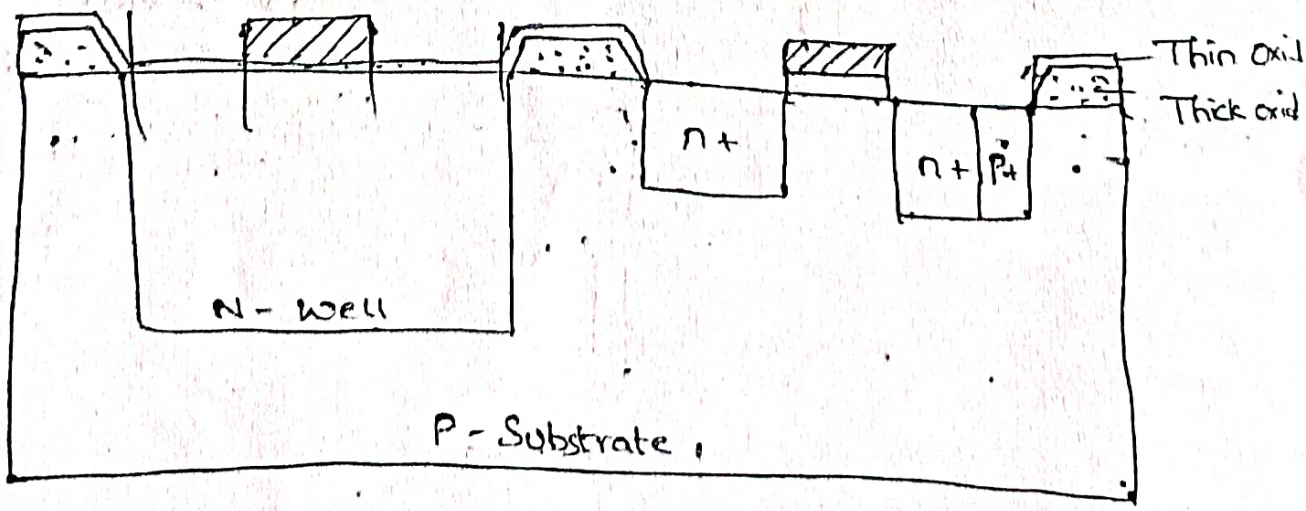


After diffusing

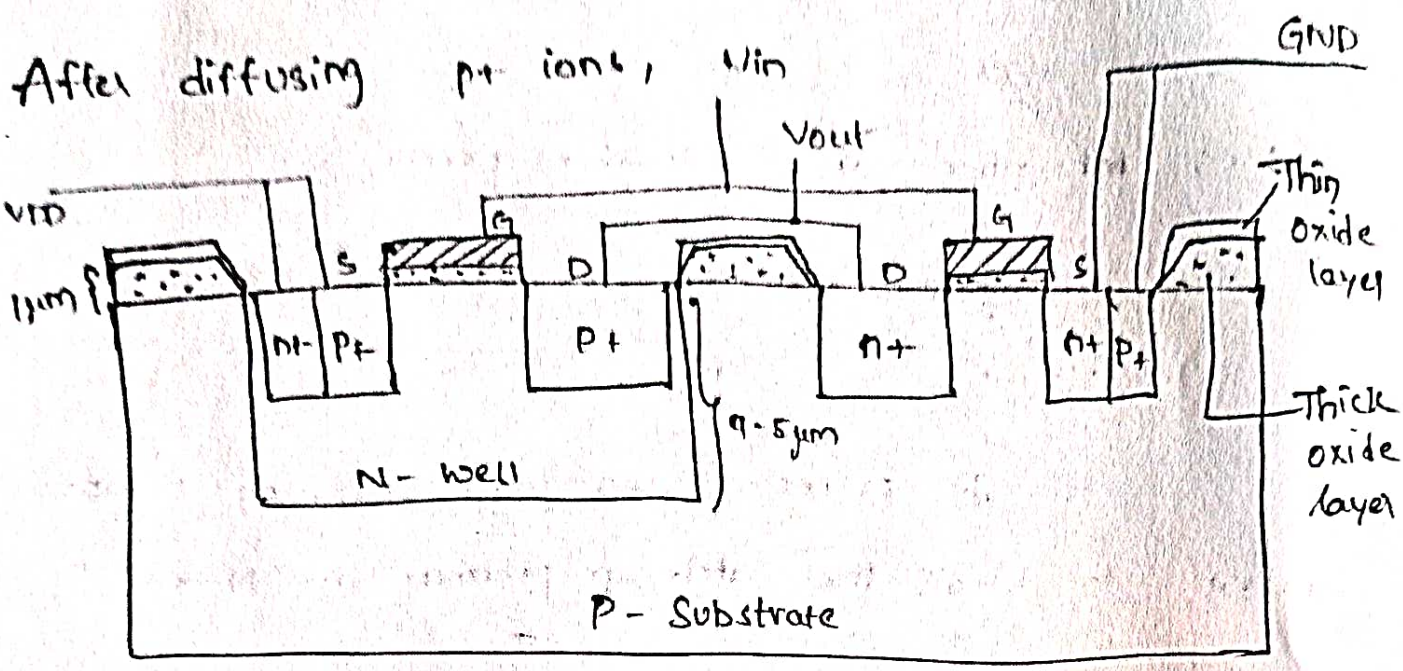


Fabricating PMOS by diffusing p+ ions in N-well through Lithography & Etching

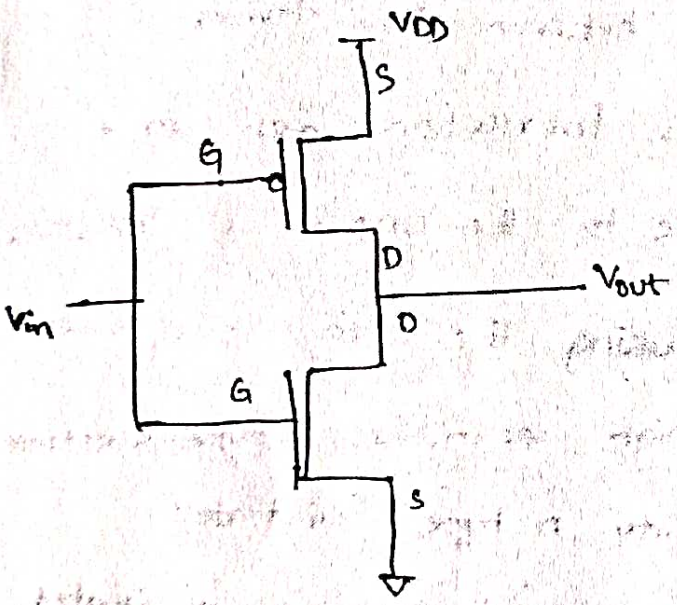


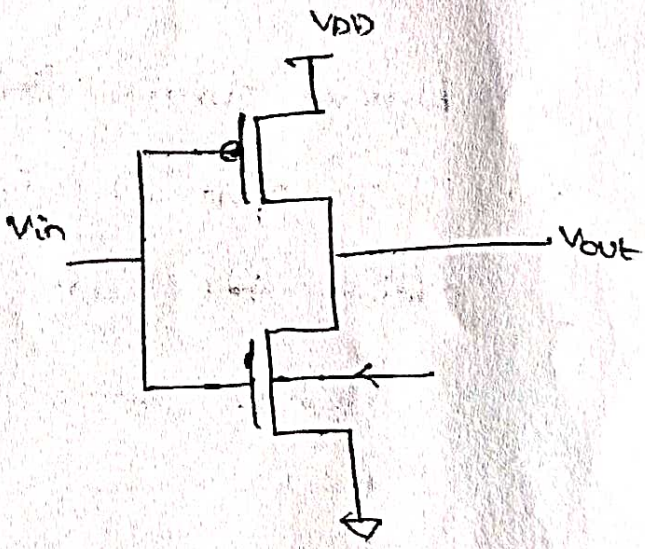


After diffusing p+ ions,



CMOS :: Circuit Diagram:





CMOS fabrication using Twintub process:-

Logical extension of the P-well and N-well processes is Twintub process.

Twin tub process uses high resistivity n-type substrate to avoid the latch up problem, in N-well & p-well process.

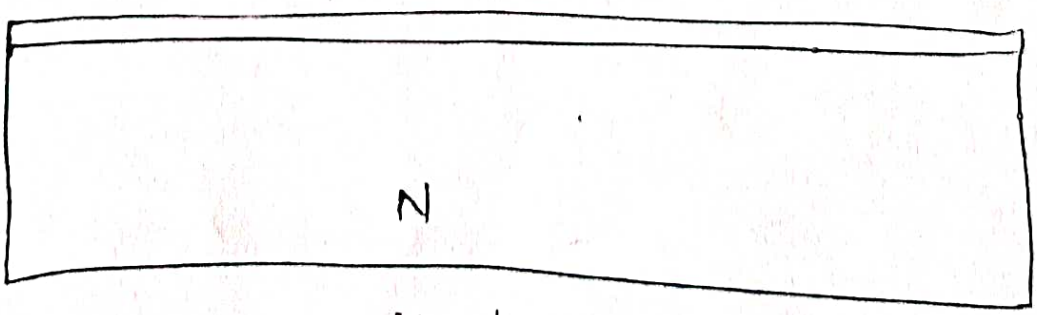
Latch-up:

Leakage current flows between the devices i.e., PMOS and NMOS in CMOS fabrication. Latch-up is a condition that occurs due to the proper well resistance

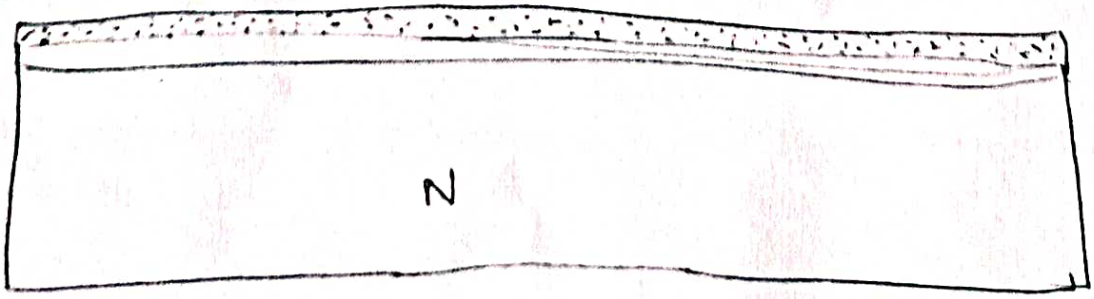
Twintub process making the both wells (N-well and P-well) on singe high resistivity n-type substrate.

1. Prepare the high resistivity n-type Substrate:

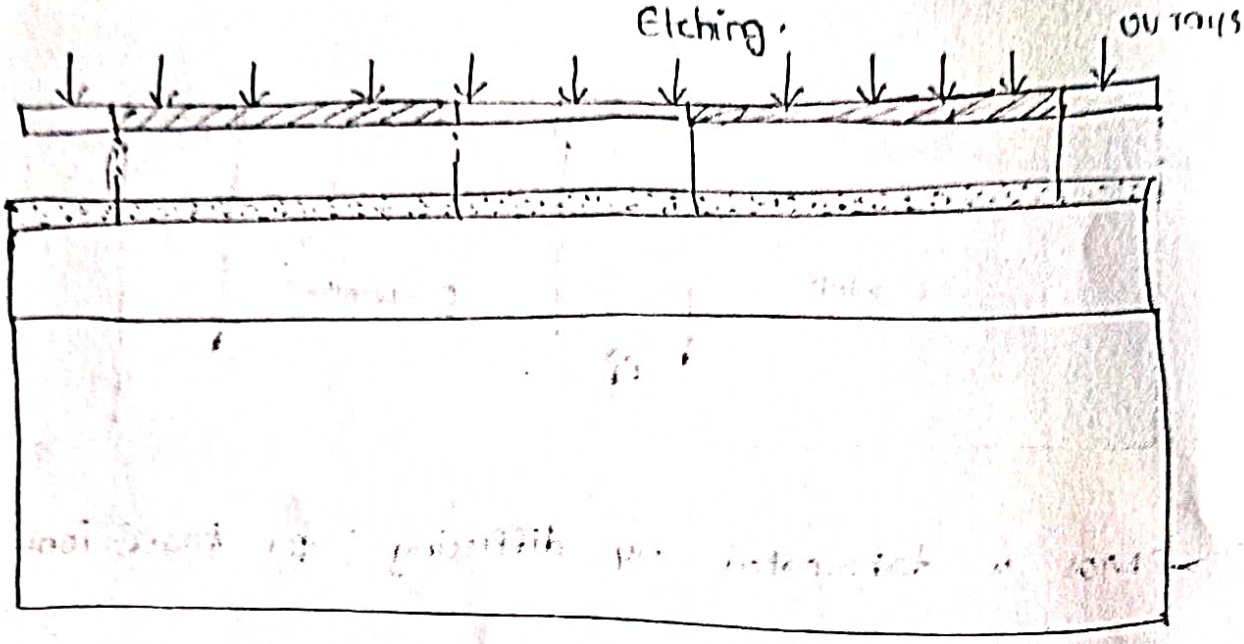
High resistivity n-type substrate layer is created by forming epi layers on the n-substrate.

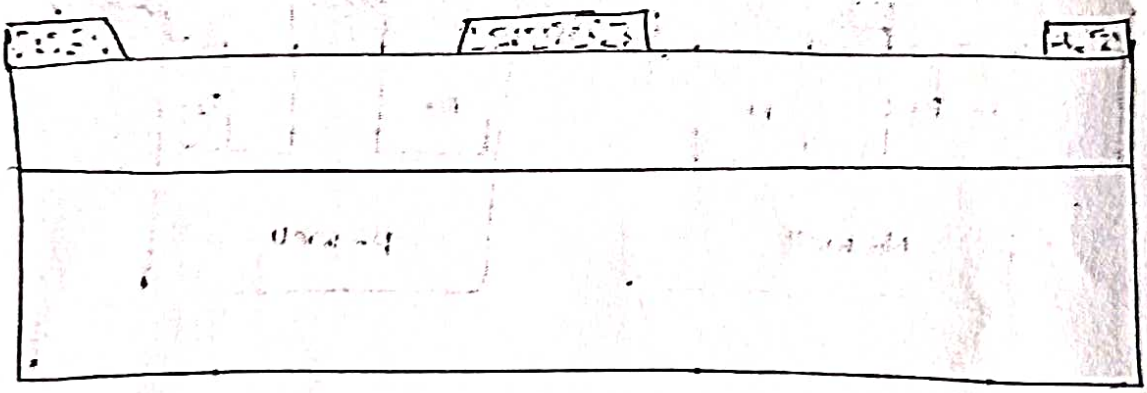


Deposition of thick oxide layer:

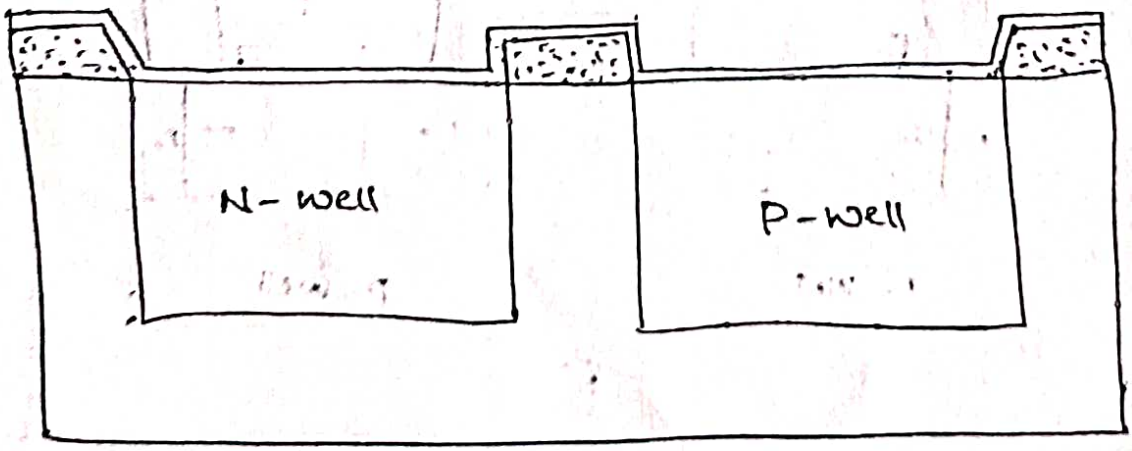


Creation of oxide window: using photo lithography and Etching.



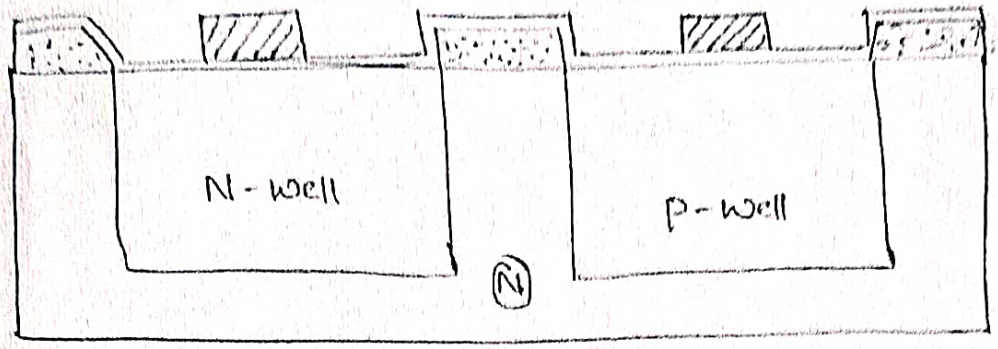


→ Creation of wells:

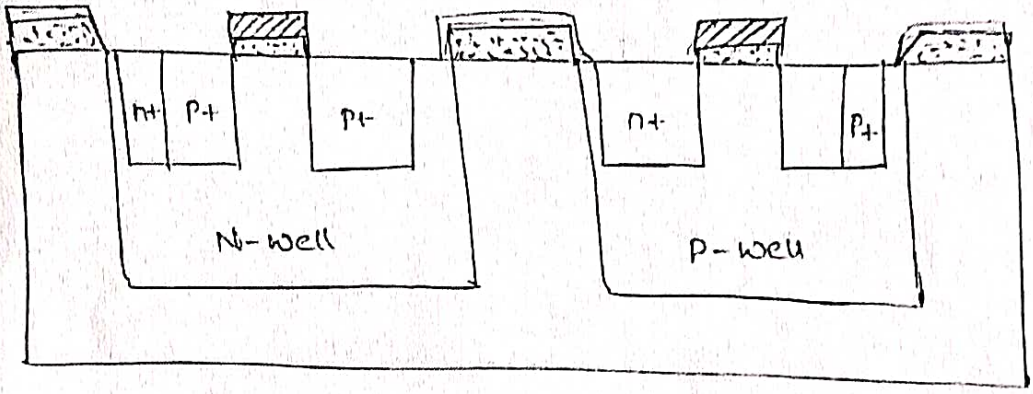


By diffusing ions, wells are created

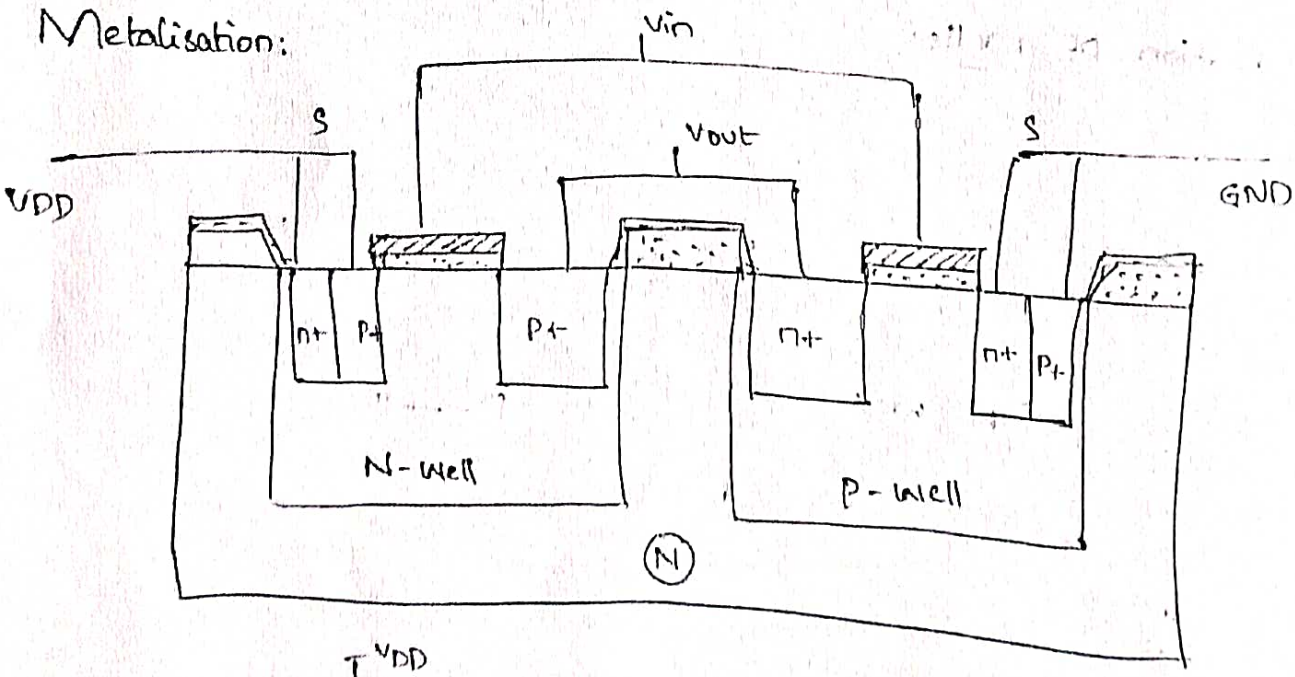
(--> pattern poly silicon is laid on the substrate

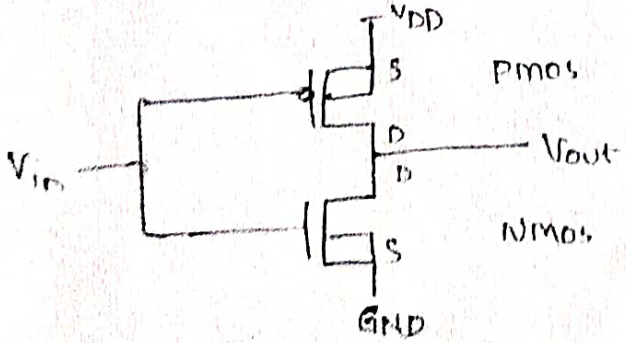


⇒ PMOS is fabricated by diffusing p+ (mask) ions



Metalisation:





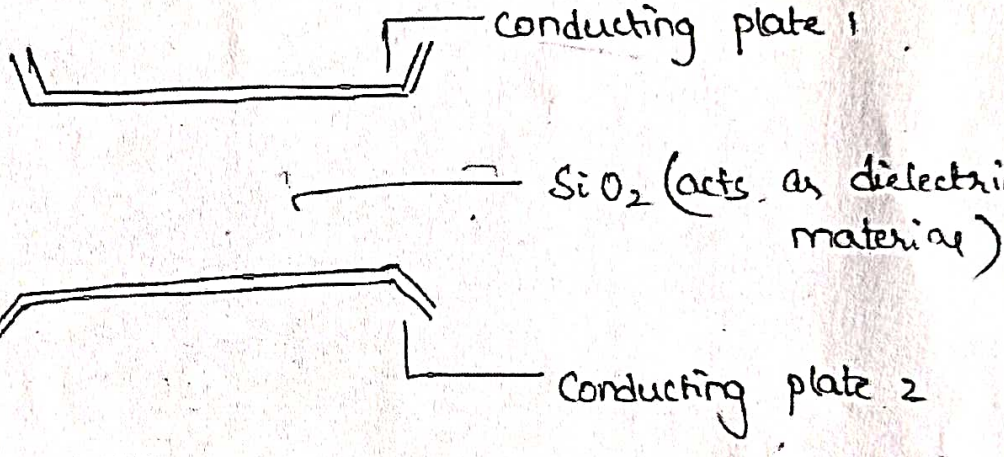
Integrated Resistors and Capacitors:

Resistors:

Three types of resistors are fabricated. They are

1. Polysilicon resistor layer (R is formed at the gate terminal by depositing the poly si layer)
2. Well resistor (R present on the well)
3. MOSFET as resistor in linear region. (or) Non-Saturated region

Capacitors:



~~Inductor:~~

poly capacitors. — b/w two poly layers depositing oxide layers.

metal capacitors. — using metal & Si

→ Inductors can't fabricate — because of larger size.

if required, made with flat metallic-thin film spirals. deposition of conduction pattern.

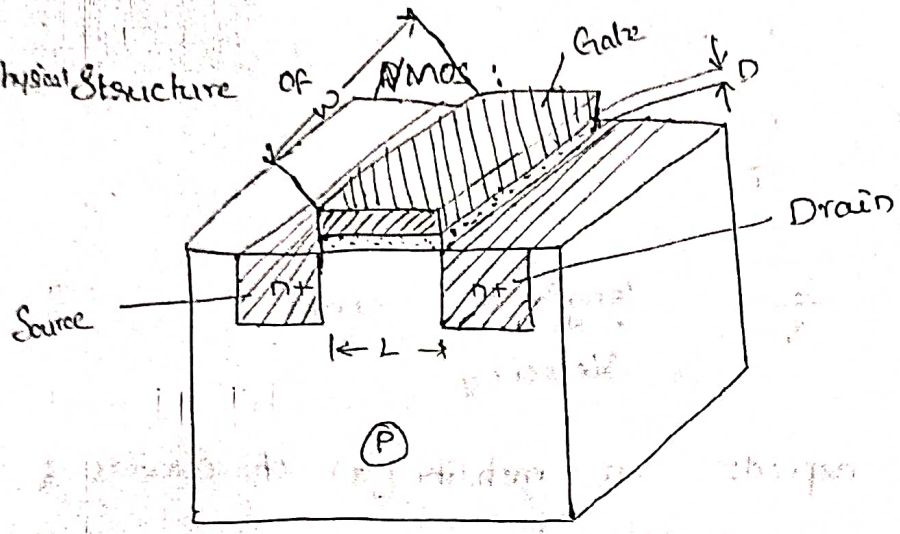
— very small inductance with set (in nano henry)

Inductors are just a wire wound ~~inductors~~ around core. integrated spiral inductors are most common.

UNIT- II

BASIC ELECTRICAL PROPERTIES (OF MOSFET)

Physical Structure of NMOS:



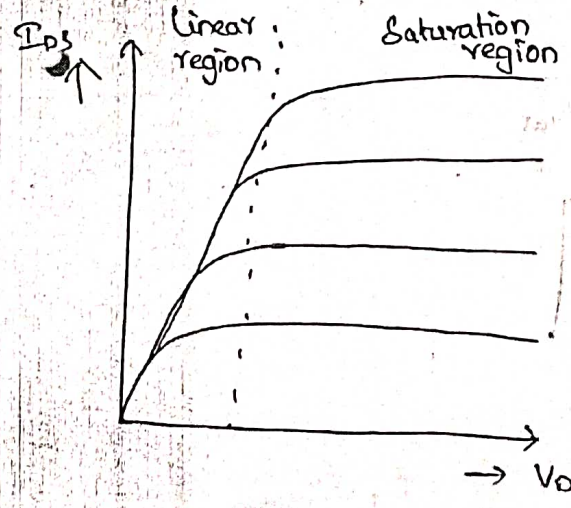
Characteristics of MOSFET:

Current I_{DS} depends both on V_{gs} & V_{DS}.

As V_{gs} ↑, the Saturation point is reached by current.

for Linear region : Effective voltage > V_{ds} ⇒ $(V_{gs} - V_t) > V_{ds}$

for Saturation region : $(V_{gs} - V_t) \leq V_{ds}$



$0.2\,V_{DD} = V_{gs}$

Current, $I = \frac{Q}{t}$

I_{ds} = Charge induced in channel (Q_c) / Electron transit time (τ)

$$I_{ds} = \frac{Q_c}{\tau}$$

But $\tau = \frac{L}{V}$ = length of channel / Velocity

Velocity depends on mobility (μ) of carriers & applied potential (E) [— E-applied Electric field]

$$\Rightarrow V = \mu E$$

Electric field, $E = \frac{V_{ds}}{L}$

$$\therefore \tau = \frac{L}{V} = \frac{L}{\mu \cdot E}$$

$$= \frac{L}{\mu \cdot \frac{V_{ds}}{L}}$$

$$\boxed{\tau = \frac{L^2}{\mu \cdot V_{ds}}}$$

Charge per unit Area; $Q = \varepsilon_0 \varepsilon_{insulator} \cdot E$

ε_0 - permitivity of free space

ε_{ins} - " " insulator

E - Electric field.

Charge per unit length of channel, $Q_c = \varepsilon_0 \varepsilon_{ins} E_g W L$

E_g - Average Electric field b/w gate to channel

ε_{ins} - relative permitivity of insulation b/w Gate to Channel

ε_0 - permitivity of free space.

W - width of the channel

L - Length of the channel.

Now, Consider Linear region,

$$E_g = \frac{V}{D}$$

$$= \frac{(V_{gs} - V_t) - \frac{V_{DS}}{2}}{D}$$

$$E_g = \frac{2V_{gs} - 2V_t - V_{DS}}{2D}$$

$$\Rightarrow Q_c = \frac{\varepsilon_0 \varepsilon_{ins} (2V_{gs} - 2V_t - V_{DS}) WL}{2D}$$

Now, $I_{ds} = \frac{Q_c}{T} = \frac{\varepsilon_0 \varepsilon_{ins} (2V_{gs} - 2V_t - V_{DS}) WL}{2D \times \frac{L}{\mu \cdot V_{DS}}}$

$$= \frac{\varepsilon_0 \varepsilon_{ins} W L}{2DL} \left((V_{gs} - V_t) - \frac{V_{DS}}{2} \right) \cdot \mu V_{DS}$$

$$\boxed{I_{ds} = \frac{\varepsilon_0 \varepsilon_{ins} \cdot \mu}{D} \cdot \frac{W}{L} \left((V_{gs} - V_t) V_{DS} - \frac{V_{ds}^2}{2} \right)}$$

Let $\frac{\varepsilon_0 \varepsilon_{ins} \cdot \mu}{D}$ is constant $= K$

$$\Rightarrow I_{DS} = K \frac{W}{L} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right)$$

$\frac{W}{L}$ is Geometric parameter

$K \cdot \frac{W}{L}$ can be represented as β

$$\Rightarrow \boxed{I_{DS} = \beta \cdot \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right)}$$

For Saturation Region,

Condition: $(V_{gs} - V_t \leq V_{ds})$

Current Eqn : $I_{ds} = \beta \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right)$

But Subsitute , $V_{ds} = V_{gs} - V_t$

$$I_{ds} = \beta \left[(V_{gs} - V_t)(V_{gs} - V_t) - \frac{(V_{gs} - V_t)^2}{2} \right]$$

$$= \beta \left[\frac{2(V_{gs} - V_t)^2 - (V_{gs} - V_t)^2}{2} \right]$$

$$I_{ds} = \beta \cdot \frac{(V_{gs} - V_t)^2}{2}$$

$$\Rightarrow \boxed{I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2}$$

Capacitance, $C = \frac{\varepsilon A}{D}$ Gate to channel Capacitance, $C_g = \frac{\varepsilon_0 \varepsilon_{ins} WL}{D}$

Gate Capacitance / Gate to channel Capacitance $= C_g$

$$C_g = \frac{\varepsilon_0 \varepsilon_{ins} WL}{D}$$

Constant, $K = \frac{\varepsilon_0 \varepsilon_{ins} \cdot \mu}{D}$ & $K = \frac{\varepsilon_0 \varepsilon_{ins} \cdot \mu}{D}$

$$K = \frac{C_g}{WL} \cdot \mu$$

$C_g = \varepsilon_0 \varepsilon_{ins} \frac{WL}{D}$

and $C_g = \frac{K}{\mu} \cdot \frac{WL}{D}$ ✗

$\frac{C_g}{WL}$

$$I_{ds} \; K = \frac{C_g \cdot \mu}{L^2} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

But $C_g = C_0 WL$

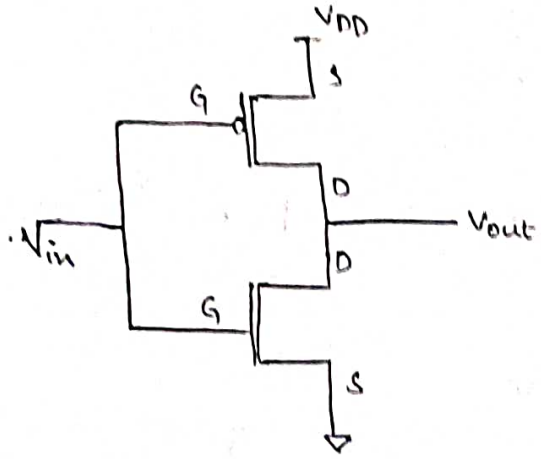
$$= \frac{C_0 WK \cdot \mu}{L^2}$$

$$I_{ds} \; K = \frac{C_0 \mu W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

15/07/15

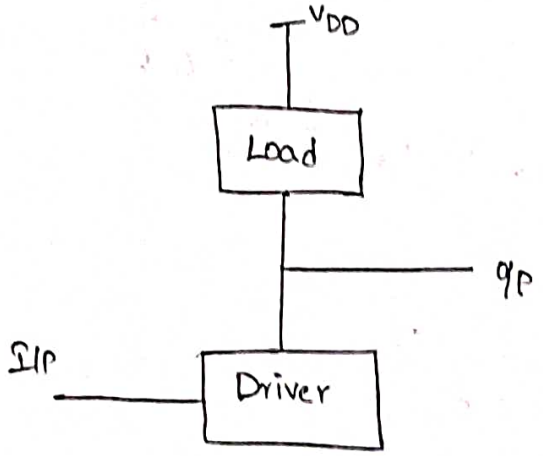
Different Inverter Configurations:

CMOS Inverter

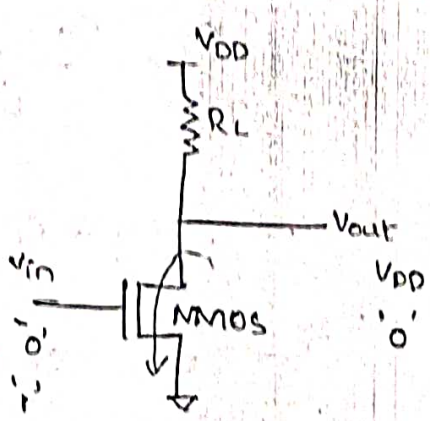


* NMOS acts as driver
Total ckt operation is dependant on NMOS
* PMOS just acts as a Load i.e., even when it is replaced by Resistor Inverter operation remains the same.

Basic Inverter Circuit:



Inverter with Resistive Load

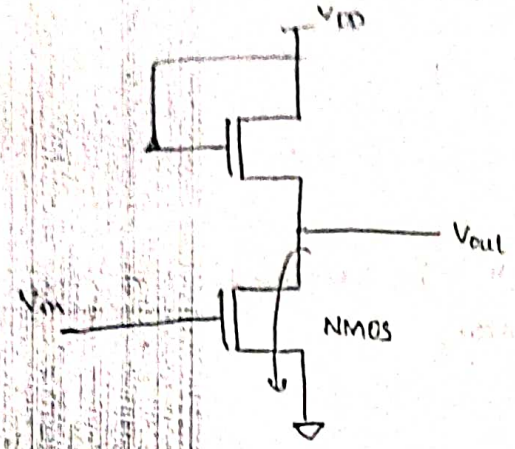


Drawbacks due to Resistive Load:

1. We cannot use diffused resistors in Integrated ckt because ——— : * It occupies more space
* It's Heat dissipation is more

* Continuously getting logic '1' at the o/p terminal so that more power is consumed / dissipated.

Inverter with Enhancement NMOS:

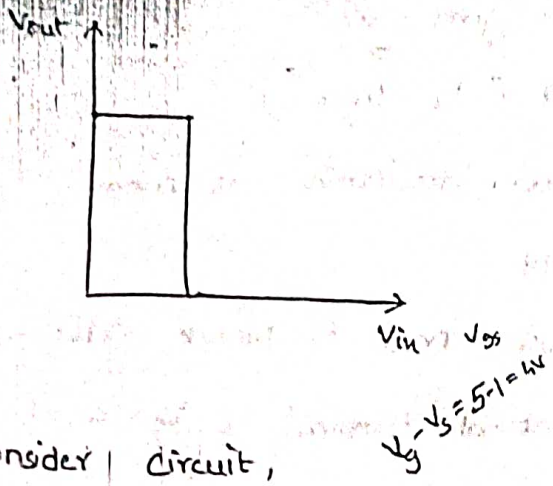


Here Enhancement NMOS is used & it is always 'ON' since its gate terminal is connected to V_{DD}.

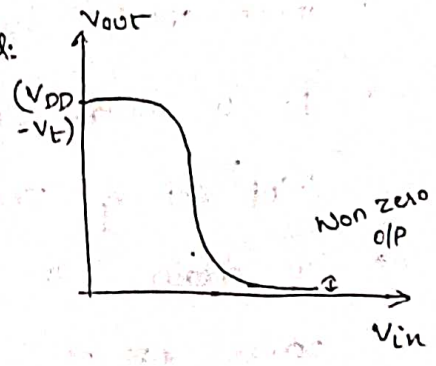
* PMOS gives strong '0'.
* NMOS gives weak '1'.
  ↳ $(V_{DD} - V_t)$ o/p

refer pass transistor logic.

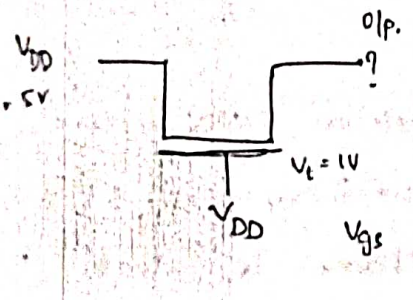
Output Waveform:

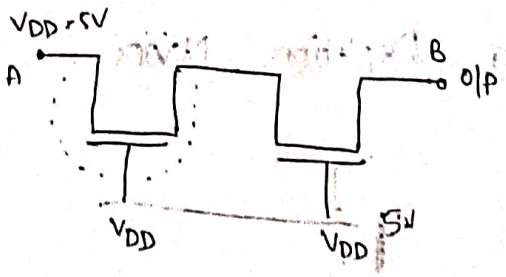


Practical:



Consider | circuit,





⇒ o/p would be 4V

$\because V_{DD} - V_t = 5 - 1 = 4V$

For 1st Transistor

V_{gs} : $V_g - V_s$

$5 - 1 = 4V$

$5 - 2 = 3V$

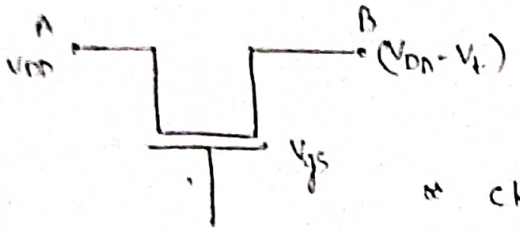
$5 - 3 = 2V$

$5 - 4 = 1V$ x device is off

//ly For second Transistor : o/p would be $V_{DD} - V_t$ = 4V//.

Pass Transistor:

-- Application of MOSFET



$V_{gs} = V_g - V_s$

$\Rightarrow$ 5 - 1 = 4V

5 - 2 = 3V

5 - 3 = 2V

5 - 4 = 1V $\Rightarrow$ device off

* ckt can be designed using pass Transistor

Drawbacks:

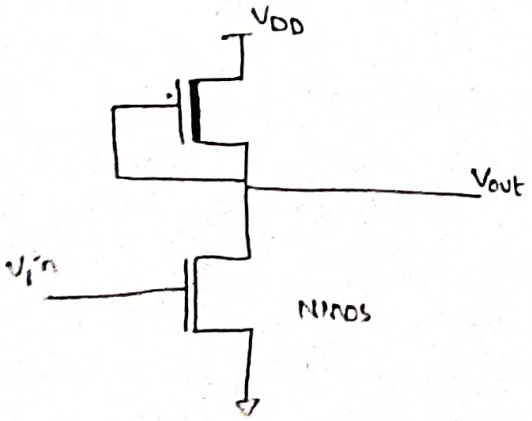
* When Enhancement NMOS is used, it is easy to fabricate but NMOS gives weak '1' i.e., we cannot obtain full swing (i.e., logic 1)

→ It is always ON $\Rightarrow$ power dissipation is more

→ Not getting zero output.

→ To obtain full swing, we need to provide additional power supplies (like at Gate terminal → $V_g = 6V$)

Using Depletion NMOS:

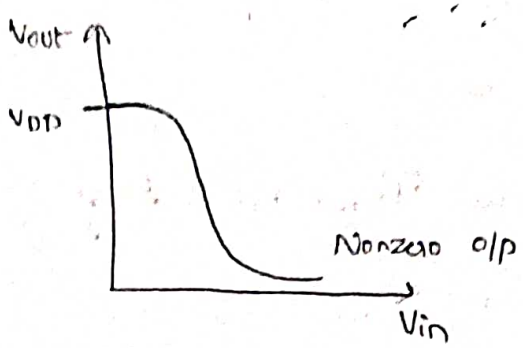


* Depletion NMOS is also continuously ON, since channel is already existing.

* We can obtain full swing but zero cant be attained since it is always ON

* Gives more current, driving capability is high

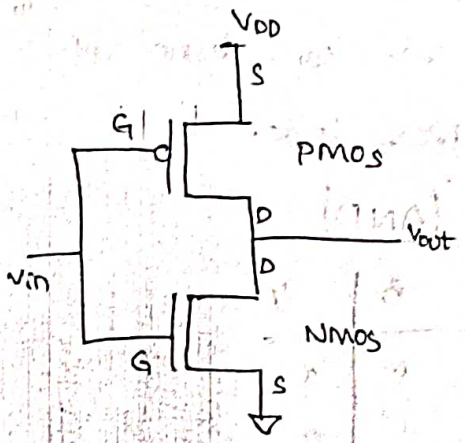
* Fast Switching.



Drawback:

- Not getting zero
  → Always ON ⇒ more power consumption

* Hence, we go for CMOS Inverter:



All the drawbacks are overcome using CMOS.

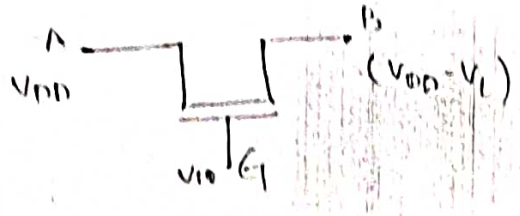
* mainly power dissipation is less
* We get full swing and also zero.

⇒ PMOS gives Strong '1'
NMOS gives Strong '0'

* To Synchronise the devices (PMOS, NMOS), the sizes are increased for PMOS since mobility of holes is less than that of e^- in NMOS. This is to obtain Symmetrical outputs.

Hence, always width of PMOS will be more.

* Power dissipation is more in case of NMOS since it is continuously in ON state



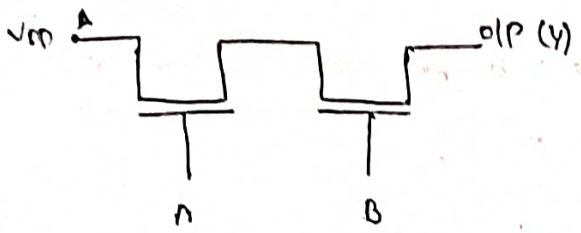
Pass Transistor Logic:

→ A Pass Transistor is one of the application of MOS Transistor (MOSFET)

→ It just pass the value from one node (A) to other node (B), acting as a switch

→ Using pass transistor logic, we can design all digital ckts similar to the CMOS logic.

Consider



AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

i) A = 0, B = 0 ⇒ Both Transistors are OFF.

⇒ Y = 0

2) A = 0, B = 0 ⇒ A is OFF & there is no path

⇒ o/p Y = 0

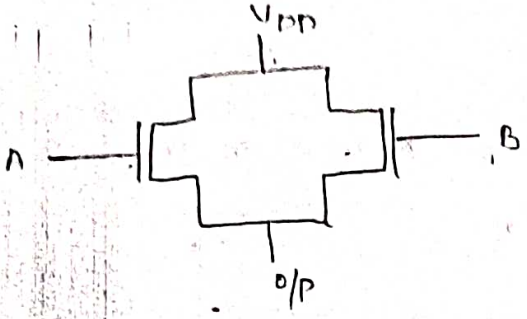
3) A = 1, B = 0 ⇒ Open ckt ⇒ o/p Y = 0

4) A = 1, B = 1 ⇒ Both are ON ⇒ o/p Y = 1

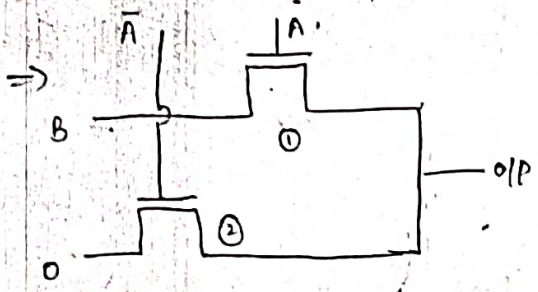
* Through CMOS we require 6 transistors for AND But here we use 2 Pass Transistors.

* Here, Pass Transistor does not give full Swing.

OR Gate:



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



⇐ AND GATE.

↳ A=0, B=0 ⇒ O/P = 0 (① is OFF, ② is ON)

→ A=0, B=1 ⇒ ① off , ② ON ⇒ O/P = 0

→ A=1, B=0 ⇒ ① ON , ② OFF ⇒ O/P = B = 0

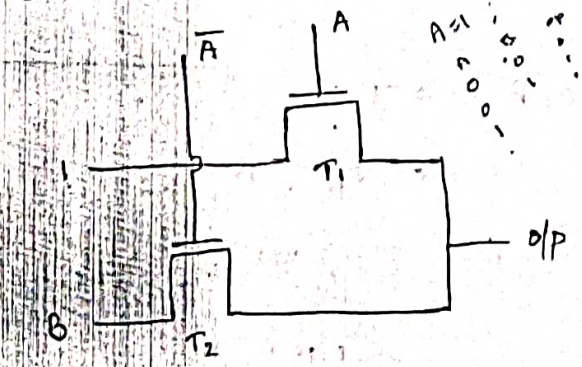
→ A=1 , B=1 ⇒ ① ON , ② OFF ⇒ O/P = B = 1

OR Gate:

A=0 ; O/P = B.

A=1 ; O/P = 1

Let A is fixed



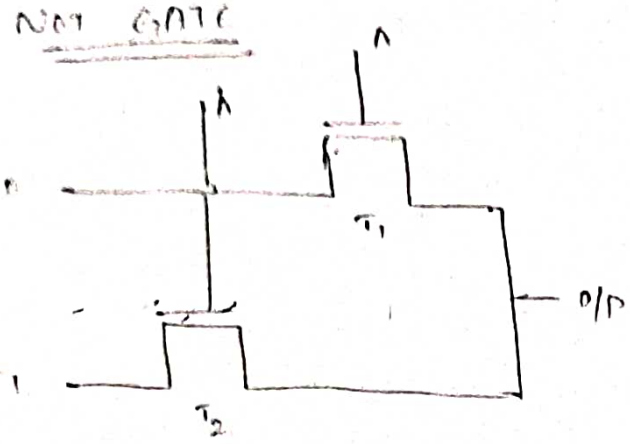
* A=0, B=0 ⇒ T_1 - OFF
  T_2 - ON
  ⇒ O/P = B = 0

* A=0, B=1 ⇒ T_1 - OFF
  T_2 - ON
  ⇒ O/P = 1 (B)

* A=1, B=0 ⇒ T_1 - ON , T_2 - OFF ⇒ O/P = 1

* A=1, B=1 ⇒ T_1 - ON , T_2 - OFF ⇒ O/P = 1

NOT GATE



A	Y
0	1
1	0

A = 0 ⇒ T_1 OFF, T_2 ON

⇒ O/P = 1

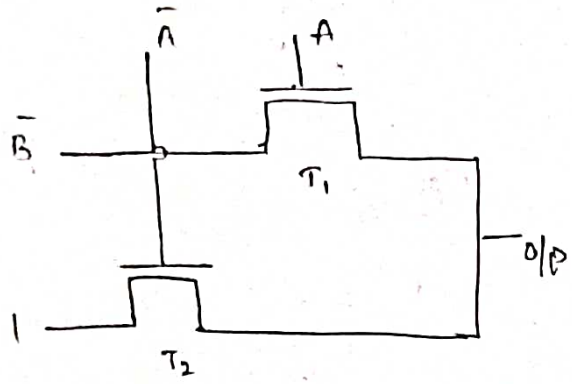
A = 1 ⇒ T_1 ON, T_2 OFF

⇒ O/P = 0

NAND GATE:

Complement of AND (Take $\bar{B}$ instead of B

1 " " 0)



A = 0, B = 0 ⇒ T_1 OFF, T_2 ON

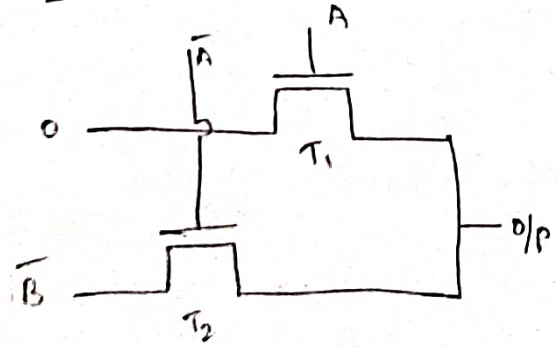
⇒ O/P = 1

A = 0, B = 1 ⇒ T_1 OFF, T_2 ON

⇒ O/P = 1

* A = 1, B = 0 ⇒ T_1 ON, T_2 OFF ⇒ O/P = $\bar{B}$ = 1
* A = 1, B = 1 ⇒ T_1 ON, T_2 OFF ⇒ O/P = $\bar{B}$ = 0

NOR GATE



A = 0, B = 0 ⇒ T_1 OFF, T_2 ON

⇒ O/P = $\bar{B}$ = 1

A = 1, B = 0 ⇒ T_1 ON, T_2 OFF

⇒ O/P = 0

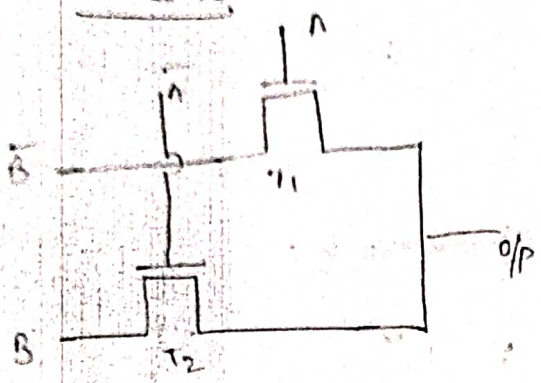
A = 0, B = 1 ⇒ T_1 OFF, T_2 ON

⇒ O/P = $\bar{B}$ = 0

A = 1, B = 1 ⇒ T_1 ON, T_2 OFF

⇒ O/P = 0

XOR GATE



A	B	Y	
0	0	0	B
0	1	1	B
1	0	1	$\bar{B}$
1	1	0	$\bar{B}$

$A=0, B=0 \Rightarrow T_2$ is ON, T_1 is OFF $\Rightarrow o/p = \bar{B} = 0$

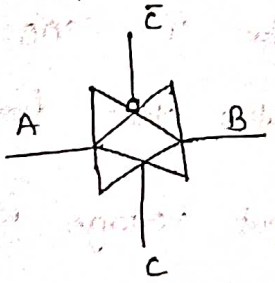
$A=1, B=0 \Rightarrow T_1$ is ON, T_2 OFF $\Rightarrow o/p = \bar{B} = 1$

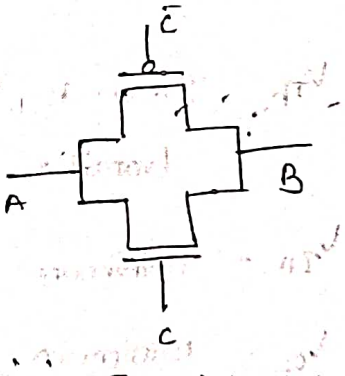
$A=0, B=1 \Rightarrow T_1$ is OFF, T_2 ON $\Rightarrow o/p = B = 1$

$A=1, B=1 \Rightarrow T_1$ ON, T_2 OFF $\Rightarrow o/p = \bar{B} = 0$.

Full Adder : Transmission gates are used to design full adder.

Transmission Gate :





* Full adder can be designed using 6 Transistors.

NAND :

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR

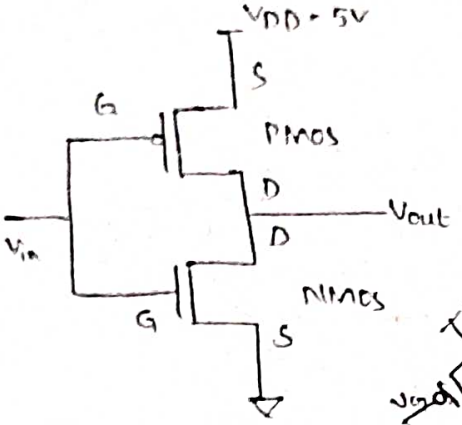
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

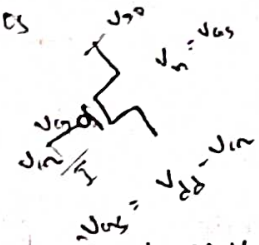
NMOS V_{DS} ↑ → Saturation region

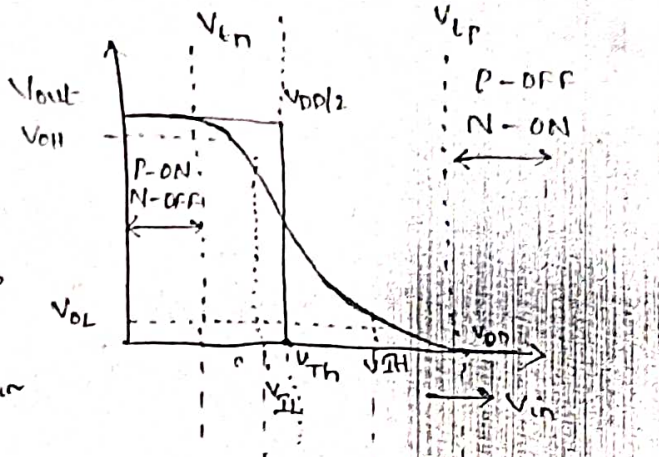
CMOS Inverter Analysis: $\left(V_{TH} = \frac{V_{DD}}{2}\right)$

CMOS Inverter:

→ Characteristics:







V_{IL} – maximum input voltage which is termed as logic '0'

V_{Th} – Threshold voltage of CMOS where the logic transition takes place from logic '1' to logic '0'.

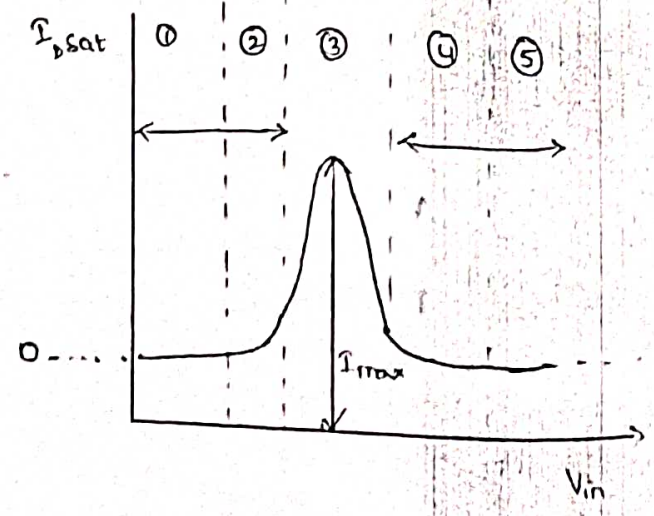
V_{IH} – minimum input voltage which is termed as logic '1'

V_{OL} – minimum output voltage which is termed as logic '0'

V_{SH} – maximum output voltage treated as logic '1'

Current Characteristics

- 3rd region in MOSFET is used as amplifier.
- remaining regions are just used as switches.



Current Characteristics:

Input	NMOS	PMOS
$V_{in} < V_{tn}$	Cut off OFF	Linear ON
$V_{in} > V_{tn}$	ON, Saturation	ON, Linear
$V_{in} = V_{th}$	ON, Sat	ON, Sat
$V_{in} < V_{DD} - V_{tp}$	ON, Linear	ON, Sat
$V_{in} \geq V_{DD} - V_t$	ON, Linear	∀ OFF

Saturation Current

NMOS — $I_{dsn} = \frac{\beta_n}{2} (V_{gsn} - V_{tn})^2$

PMOS — $I_{dsp} = \frac{\beta_p}{2} (V_{gsp} - |V_{tp}|)^2$

20/07/18

In

* Region ① and ⑤, only one of the Transistor is ON [① → PMOS ON ⑤ → NMOS ON]. So that there is no current flow blw the power rails (V_{DD} & GND)

NOTE: Region ① - PMOS is ON ; NMOS - OFF

Region ⑤ - PMOS is OFF ; NMOS - ON

Similarly

In Region ②, PMOS is operating in linear region. NMOS is operating in Saturation region.

Currents:

$\beta_n = 0 \frac{W_n}{L_n}$

$\beta_p = \frac{W_p}{L_p}$ $\beta_n = \frac{W_n}{L_n}$

For PMOS (Linear),

$$I_{DSP} = \underbrace{K_p \frac{W_p}{L_p}}_{\beta_p} \left((V_{gs} - V_{tp}) V_{dsp} - \frac{V_{dsp}^2}{2} \right)$$

For NMOS (Saturation),

$$I_{dsn} = \underbrace{K_n \frac{W_n}{L_n}}_{\beta_n} \frac{(V_{gsn} - V_{tn})^2}{2}$$

Amount of current can be calculated by equating these two equations.

* In region ③ both transistors are in Saturation region

$$I_{DSP} = \frac{\beta_p}{2} (V_{gsp} - V_{tp})^2$$

$$\therefore (V_{in} - V_{DD}) - V_{tp}$$

$$I_{dsp} = \frac{\beta_p}{2} (V_{in} - V_{DD} - V_{tp})^2$$

$$I_{DSN} = \frac{\beta_n}{2} (V_{gsn} - V_{tn})^2$$

$$\boxed{I_{DSN} = \frac{\beta_n}{2} (V_{in} - V_{tn})^2}$$

* Since in saturation, both currents are equal & maximum.

V_{in} can be obtained by equating them.

$I_{dsp} = I_{dsn}$

$$\frac{\beta_p}{2}(V_{in} - V_{DD} - V_{tp})^2 = \frac{\beta_n}{2}(V_{in} - V_{tn})^2$$

$$\beta_p\left[V_{in}^2 + V_{DD}^2 + V_{tp}^2 - 2V_{in}V_{tp} + 2V_{DD}V_{tp} - 2V_{in}V_{tp}\right] = \beta_n(V_{in} - V_{in})^2$$

$$V_{in} = \frac{V_{DD} + V_{tp} + V_{tn}\left(\frac{\beta_n}{\beta_p}\right)^{1/2}}{1 + \left(\frac{\beta_n}{\beta_p}\right)^{1/2}}$$

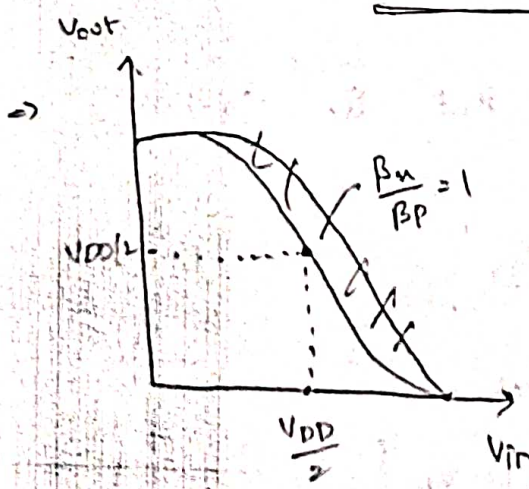
Considering $\beta_n / \beta_p \Rightarrow \frac{\beta_n}{\beta_p} = 1$

$$\Rightarrow V_{tn} = -V_{tp}$$

$$\therefore V_{in} = \frac{V_{DD} + V_{tp} + (-V_{tp})(1)^{1/2}}{1 + (1)^{1/2}}$$

$$= \frac{V_{DD} + V_{tp} - V_{tp}}{1+1}$$

$$V_{in} = 0.5\,V_{DD}$$



But practically it is not possible to have $\frac{\beta_n}{\beta_p} = 1$

$\mu_p = 2.5\mu_n$

$$\frac{W_p}{L_p} = 2.5\frac{W_n}{L_n}$$

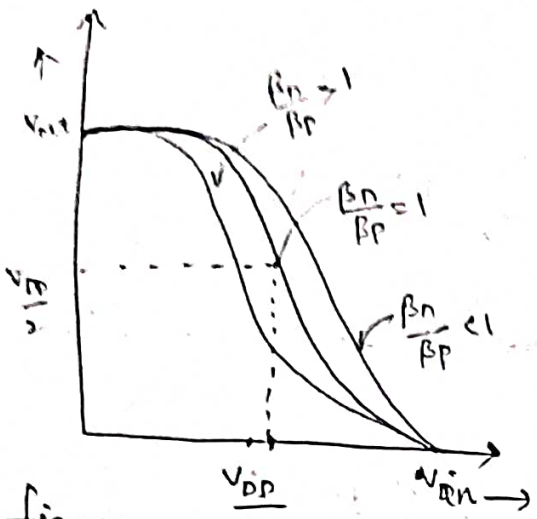


figure:

figure

Transfer Characteristics with β ratio

Trans Conductance (g_m) & Output Conductance (g_{ds}):

These are performance parameters of a device.

Trans conductance is the relation b/w the output current (I_{DS}) to input Voltage (V_{gs})

$$\Rightarrow g_m = \left.\frac{\partial I_{DS}}{\partial V_{gs}}\right|_{V_{ds} = \text{constant}}$$

* A good device must have high Trans conductance.

In terms of circuit parameters,

$$I_{ds} = \frac{Q_c}{\tau} \qquad \text{But} \quad Q_c = C_g \cdot \partial V_{gs}$$

$$\tau = \frac{L^2}{\mu V_{ds}}$$

$$\therefore g_m = \frac{\partial I_{DS}}{\partial V_{gs}} = \frac{C_g \cdot \partial V_{gs}}{\frac{L^2}{\mu V_{ds}}} \cdot \frac{1}{\partial V_{gs}}$$

$$\boxed{g_m = \frac{C_g \cdot \mu \cdot V_{ds}}{L^2}}$$

C_g - Gate Capacitance, $\frac{\varepsilon_0 \varepsilon_{ins} W L}{D}$

$$\Rightarrow g_m = \frac{\varepsilon_0 \varepsilon_{ins} W L \cdot \mu \cdot V_{ds}}{L^2 \cdot D}$$

$$g_m = \frac{\varepsilon_0 \varepsilon_{ins} W \mu V_{ds}}{L \cdot D}$$

$$g_m = \underbrace{\frac{\varepsilon_0 \varepsilon_{ins} \cdot \mu}{D}}_{\beta} \cdot \frac{W}{L} \cdot V_{ds}$$

$g_m = \beta V_{ds}$.

In saturation $V_{ds} = (V_{gs} - V_t)$

$g_m = \beta (V_{gs} - V_t)$

can't be changed (∵ Geometric parameters)

To improve g_m W must be ↑ - But size is ↑. otherwise L ~~is~~ length of channel can be ↓. But it is technology dependant & also o/p resistance ↑, Gain ↓.

$$\therefore R_{ds} = \frac{1}{g_{ds}}$$

Smaller g_{ds} increase the voltage gain, which is benficial for analog & digital ckt applications.

$$g_{ds} = \frac{\partial I_{DS}}{\partial V_{gs}} \qquad g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}}$$

Threshold Voltage:

It is the voltage at which conduction will start

$$V_t = \phi_{ms} \frac{Q_B - Q_{ss}}{C_0} + 2\phi_{fN}$$

Q_B = Charge per unit area in the depletion layer beneath the oxide.

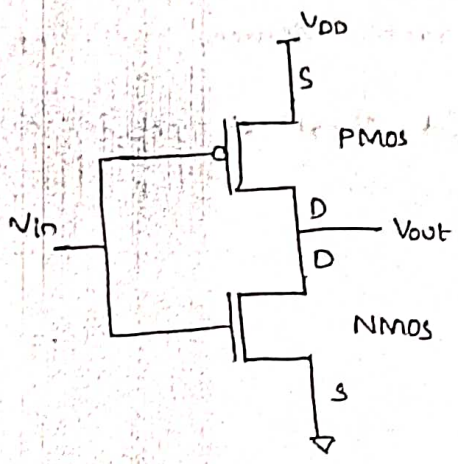
Q_{ss} = Charge density at Si : SiO_2 Interface.

Solution:

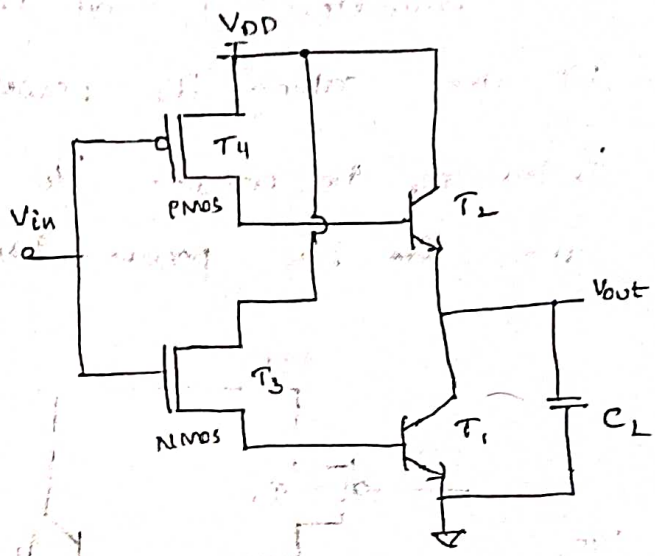
Bi CMOS Inverter: It is the combination of BJT & CMOS Technology.

CMOS Technology	BJT Technology
1. I/p Impedance is high (compared to BJT)	1. I/p impedance is low
2. Power Consumption is less	2. Power consumption is high.
3. High packing density i.e., Small in size & more components can be accomodated	3. Packing density is low
4. Easy to Fabricate	
5. Flexibility - Source, drain terminals can be changed.	
6. Propagation delay is small i.e., High speed.	
7. Less o/p current so that driving capability decreases	7. High o/p current $\Rightarrow$ High driving capability.

Bi CMOS Inverter:



CMOS Inverter



Bi CMOS Inverter

When $V_{in} = 0$,

T_4 is ON, T_2 is ON, output is $V_{out} = V_{DD}$

i.e., logic (1)

Similarly When $V_{in} = 1$,

T_3 is ON (NMOS), T_1 is ON, output is 0

Advantages:

→ Input Impedance is high

→ O/p current is high & hence driving capability is high

→ Voltage levels are (term) good

Drawbacks:

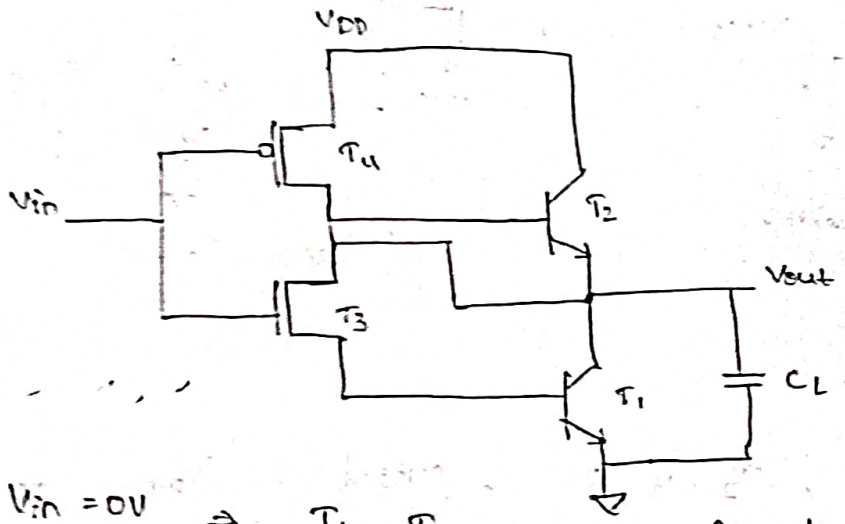
→ More no. of components are used.

→ Size is more

∴ Used for High Speed Applications with no space constrain

→ There is a path existing b/w the power rails and Transistors T_3 and T_1 so that unnecessarily, we are calling the power from source i.e., V_{DD}.

Redrawing the circuit: (to avoid short ckt power dissip. ation ~~for~~ b/w power rails)



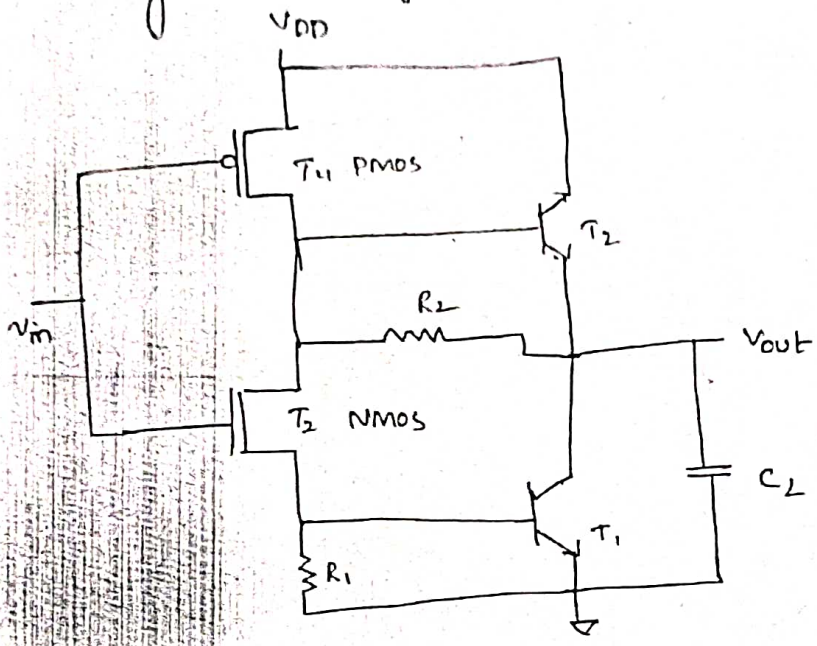
$V_{in} = 0V \Rightarrow T_4, T_2$ are ON & o/p = 5V (logic ①)

for logic ①, T_3 is ON & the voltage from T_2 o/p (5V) is given as input to T_1 through T_3 (ON) & the voltage is discharged. Thus o/p = '0' logic

Based on the Threshold voltage of the BJT, the voltage gets discharged upto more than Thresh. voltage. Hence, we don't get full swing.

* Here we are adding another discharge path To drain/discharge the remaining voltage present at the Base terminal of T_1 & to avoid full voltage problems.

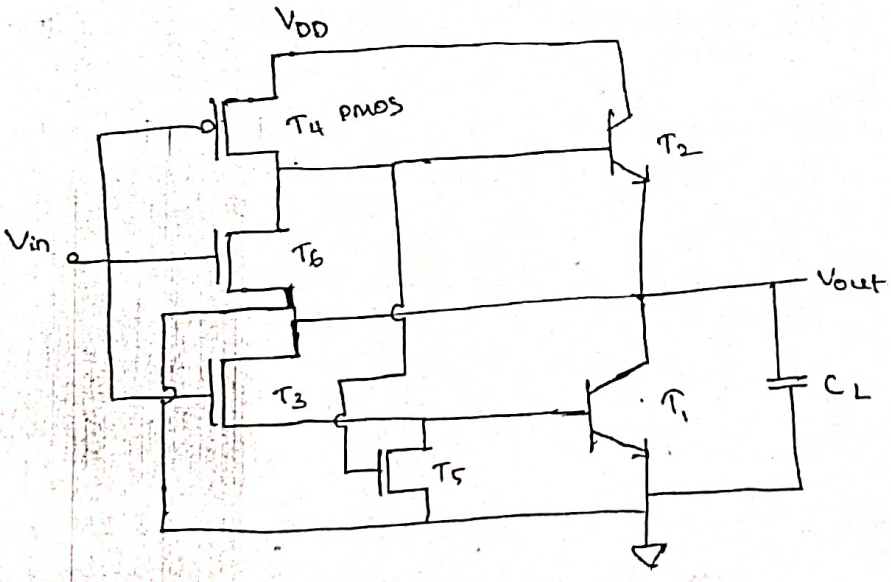
Redrawing ckt, we get



∴ Resistors can't be used in the Digital Integrated ckts.

Hence Resistors must be modified / replaced by MOS Transistors

Again redrawing ckt,



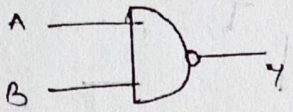
When $V_{in} = 0$, T_4, T_2, T_5 are ON ⇒ o/p = logic 1

31/07/18

UNIT - III

VLSI Circuit Design Flow

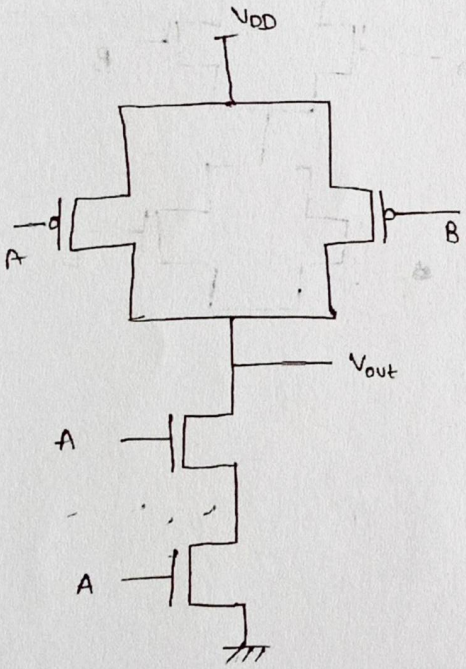
NAND GATE



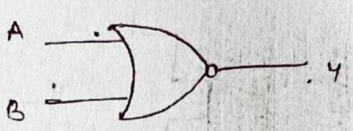
$Y = \overline{AB}$

AB - NMOS

A+B - PMOS



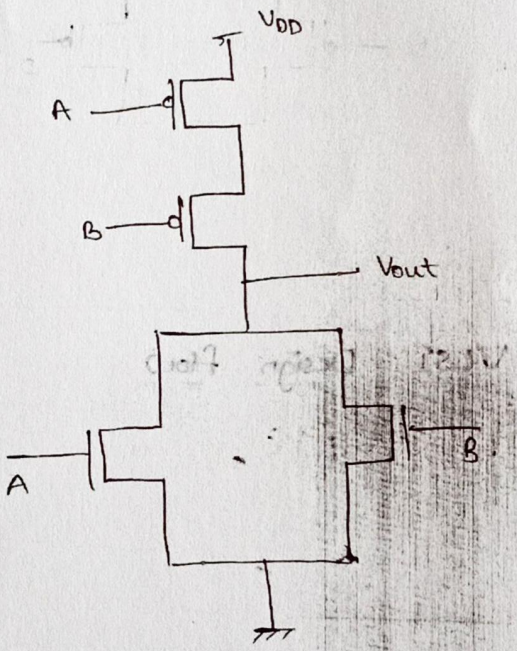
NOR GATE



$Y = \overline{A+B}$

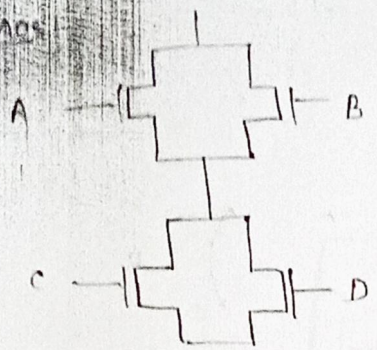
A+B - NMOS

AB - PMOS

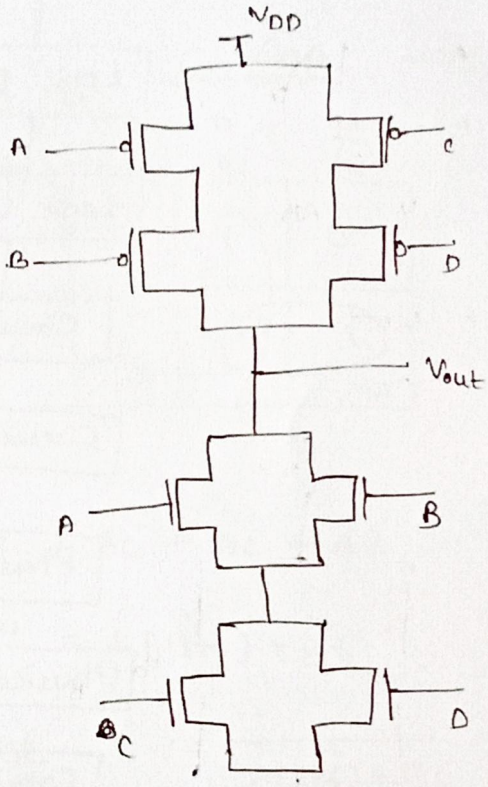


Design the circuit $\overline{(A+B)(C+D)}$

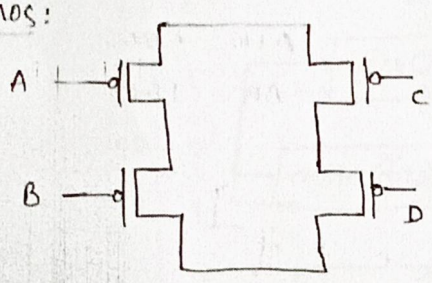
NMOS:



$\overline{(A+B)(C+D)}$



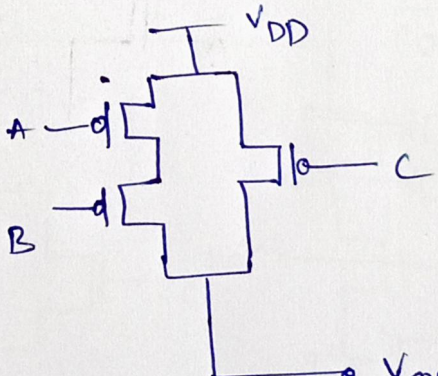
PMOS:



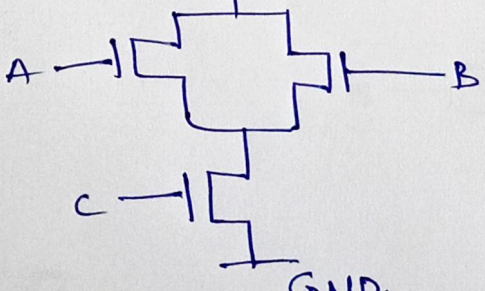
VLSI Design Prob.

$F = \overline{(A+B)C}$

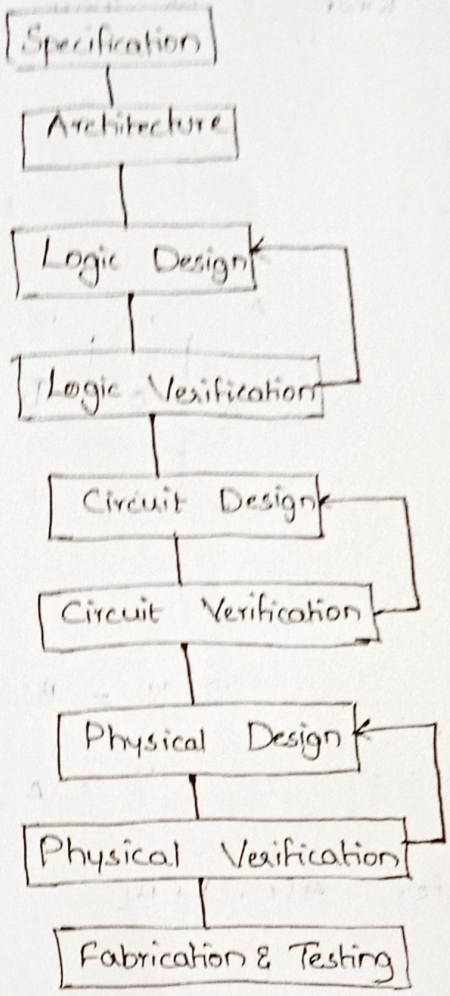
PMOS:-



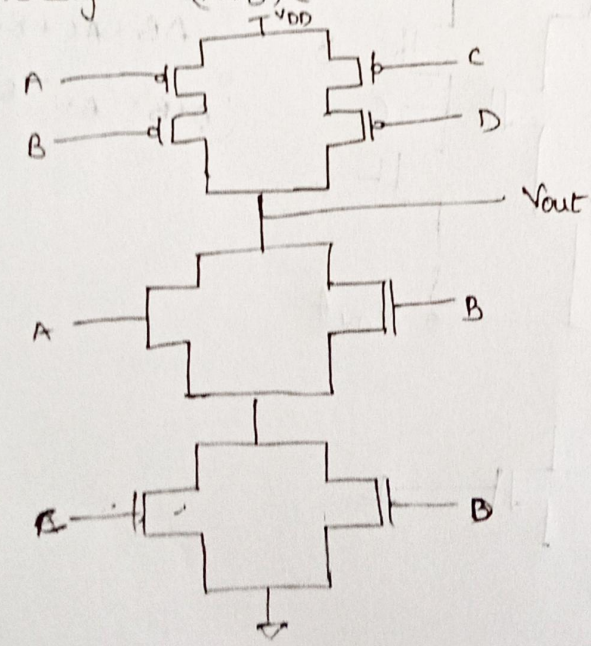
NMOS:-



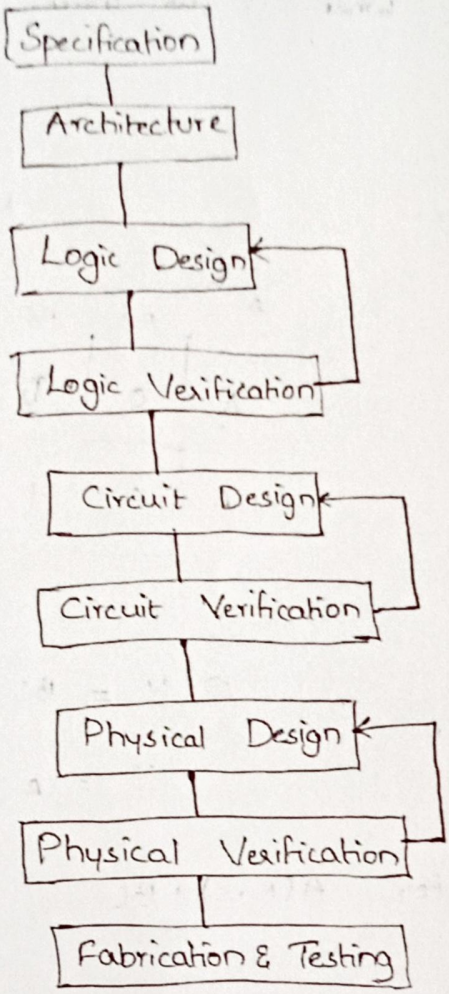
VLSI Design Flow:



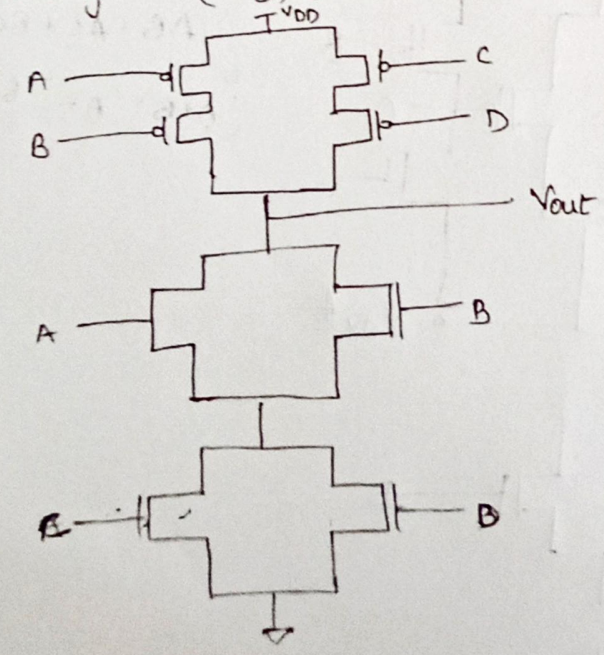
Design $\overline{(A+B)(C+D)}$



VLSI Design Flow:



Design $\overline{(A+B)(C+D)}$



* Design a circuit which contains 3 i/ps & one o/p.
The o/p is '1' when 2 or more i/ps are high one

Truth Table

A (X)	B (Y)	C (Z)	o/p (F)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

K - Map

A \ BC	$\bar{B}\bar{C}$ (00)	$\bar{B}C$ (01)	BC (11)	$B\bar{C}$ (10)
$\bar{A}$	0	0	1	0
A	0	1	1	1

$\Rightarrow Y = BC + AC + AB$

$Y = A(B+C) + BC$

CMOS ckt for $A(B+C)' + BC$

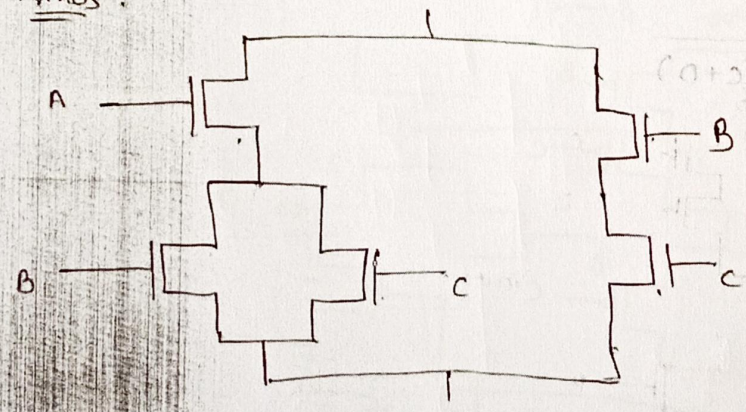
$\overline{A(B+C) + BC}$

$\overline{A} + \overline{BC}$

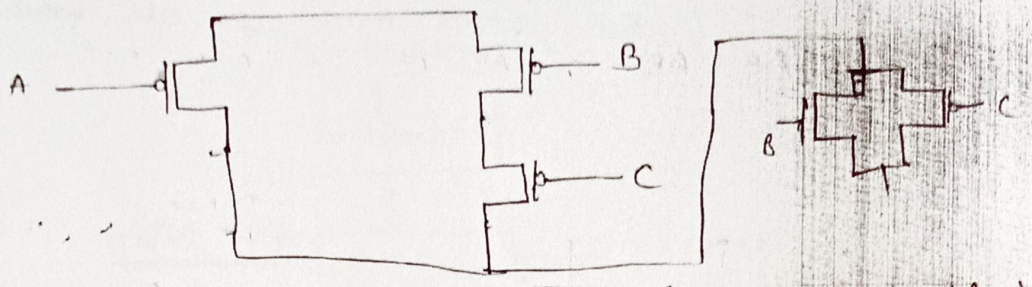
$AB + AC + BC$

$(A+B)(A+C)(B+$

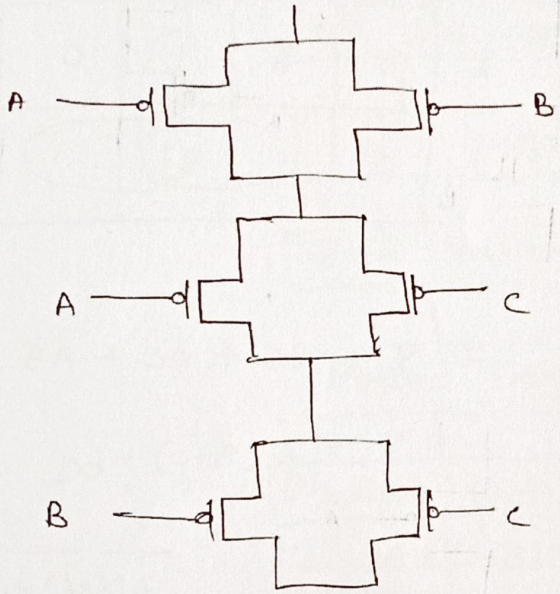
NMOS :



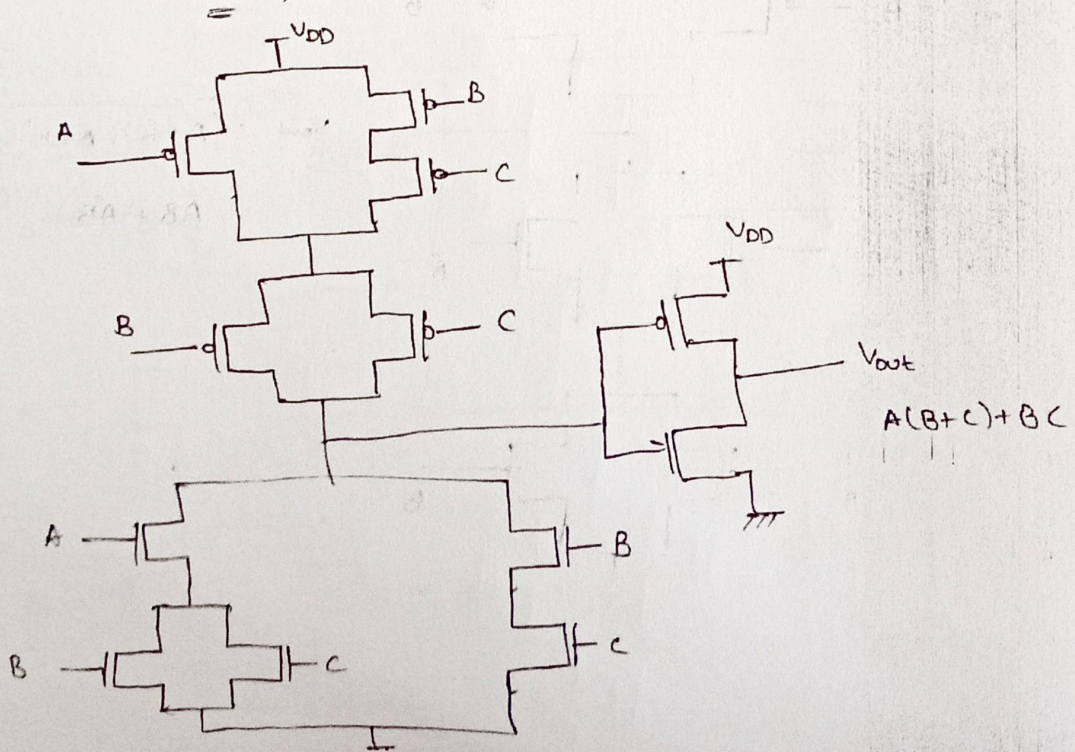
PMOS complimented form: $A+(BC)(B+C)$



PMOS for comp form $\overline{A(B+C)+BC} = (A+B)(A+C)(B+C)'$



Ckt for $A(B+C)+BC$



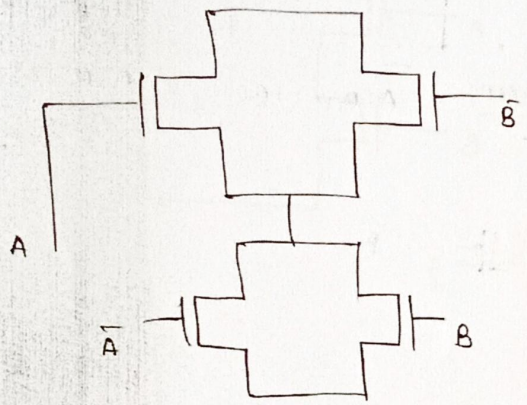
$\bar{A} = A$

4

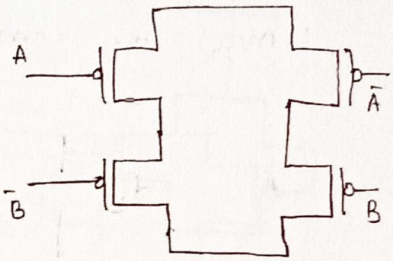
XOR Gate

$$Y = \bar{A}B + A\bar{B} = \overline{\bar{A}B + A\bar{B}} = \overline{(A+\bar{B})(\bar{A}+B)}$$

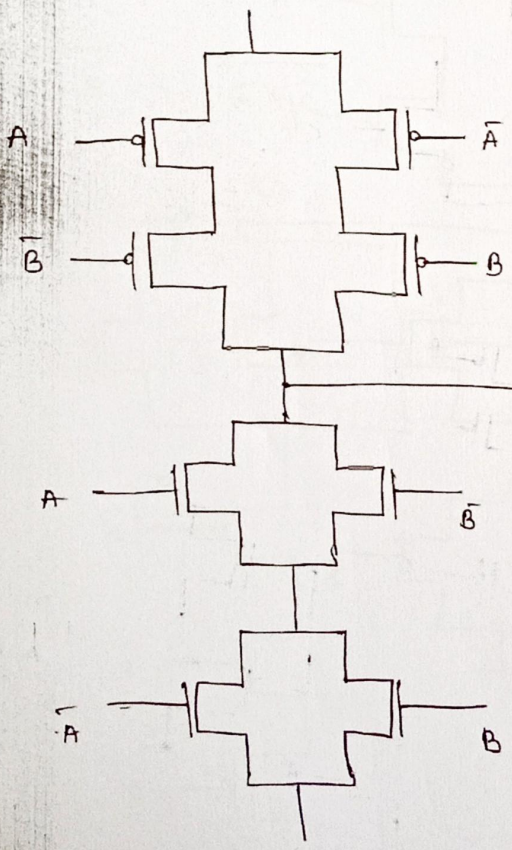
NMOS:



PMOS



XOR Gate:



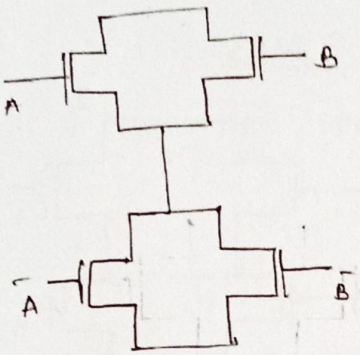
Vout : $\overline{(A+\bar{B})(\bar{A}+B)}$

$= \bar{A}B + A\bar{B}$

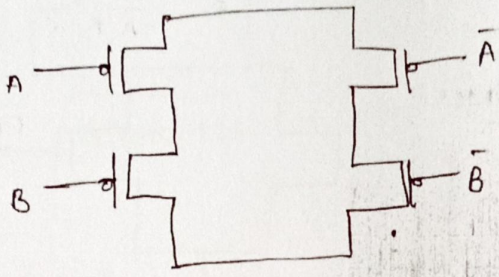
XNOR GATE:

$$Y = \bar{A}\bar{B} + AB = \overline{\bar{A}\bar{B} + AB} = \overline{(A+B)(\bar{A}+\bar{B})}$$

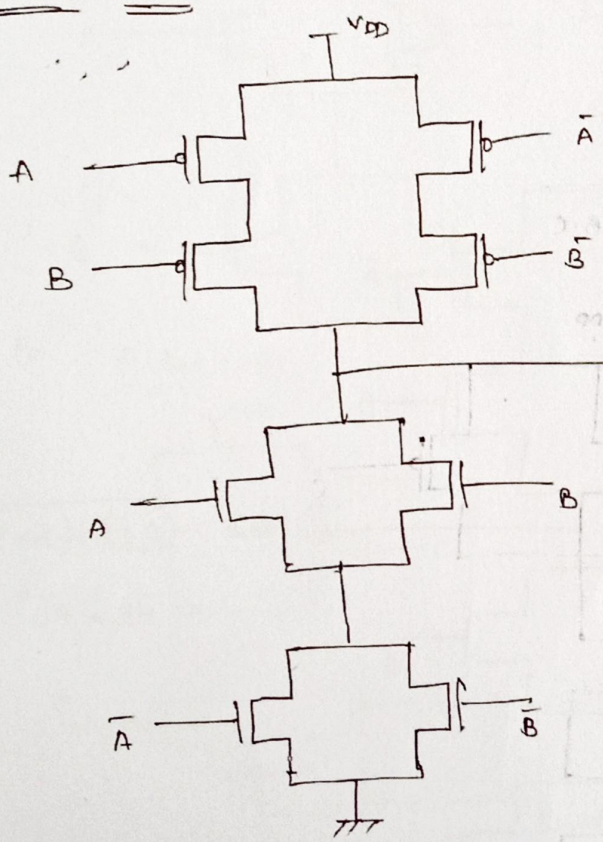
NMOS:



PMOS:



XNOR Gate:



V_{OUT} : $Y = \overline{(A+B)(\bar{A}+\bar{B})}$

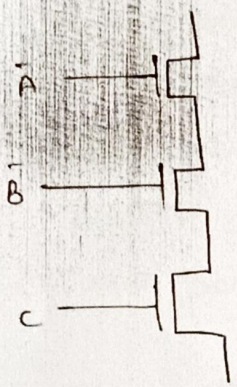
$= \bar{A}\bar{B} + AB$

Design ckt $Y = \overline{(A+B)\cdot C} = (A+B)\bar{C}$ ... AB...

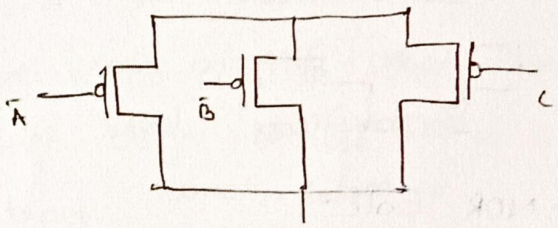
$= \overline{\bar{A}\bar{B} + \bar{C}}$

$= \overline{\bar{A}\cdot\bar{B}\cdot C}$

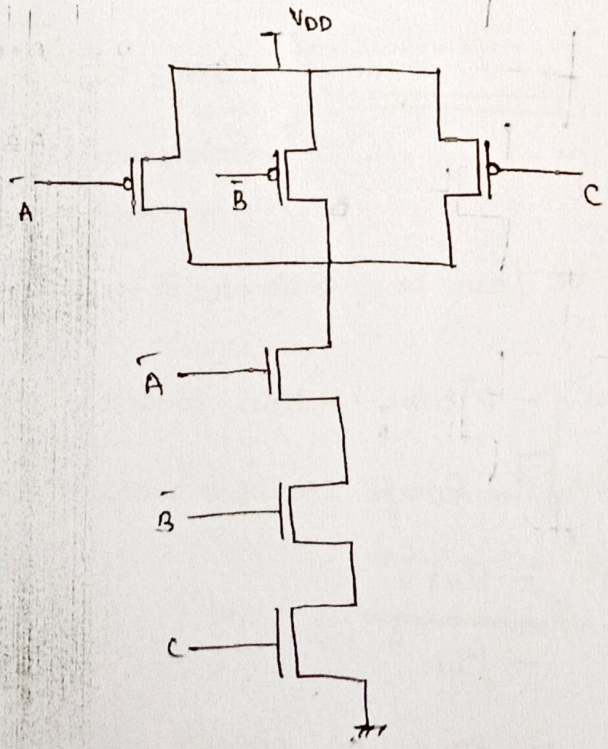
NMOS:



PMOS:



$Y = \overline{(A+B)\cdot C} = \overline{\bar{A}\cdot\bar{B}\cdot C}$



02/08/18

LAYOUT : Physical design of the circuit.

* Layout is the actual circuit which we are placing on a substrate or wafer.

→ 4 layers in MOS Technology

→ There are 4 types of MOS Layers

1. P - diffusion layer < for designing P-MOS>
2. N - diffusion layer < for designing N-MOS>
3. polysilicon layer < for designing Gate>
4. metal layer. < for routing purpose>

All the layers are isolated with thin oxide layer or thick oxide layer.

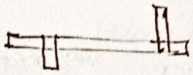
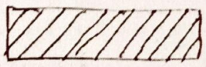
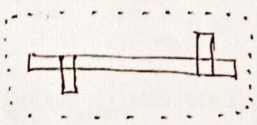
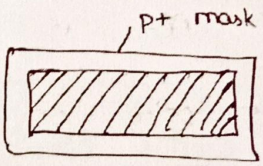
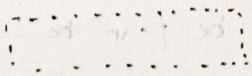
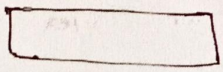
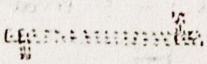
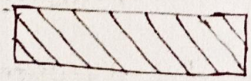
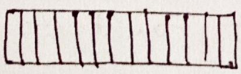
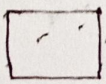
* P - diffusion layer represents PMOS
* N - " " " NMOS
* polysilicon " " GATE Terminal of device.
* Metal " " Interconnections & routing information

Each layer will be / can be designated or identified by colours

1. P diffusion layer } - P^+ mask - Yellow to identify PMOS
2. N diffusion layer } Green colour layers.
3. Polysilicon layer - Red
4. Metal layer - Blue

* Contact is used to connect 2 layers which is black in colour

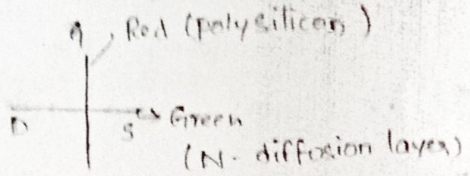
* Stick Diagrams: It is a planning of layout before designing the actual physical design. It is also called the rough diagram / blue print of layers.
* Stick diagram gives the layers information & routing (interconnection) information for better design of layout.
* In Stick diagram, there is no need to follow the Geometric dimensions of design because it is a rough diagram of layout.

Layer	Colour	Stick Symbol	Layout Symbol
1. N-diffusion	Green		
2. P-diffusion	Green with pt mask		
3. pt mask	Yellow		
4. Polysilicon	Red		
5. Metal	Blue		
6. Contacts	Black		
7. Implant	Yellow		

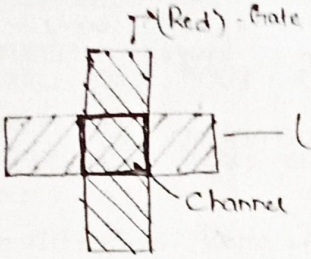
Transistor Design:

(No dimensions for stick diag)

NMOS: Stick diagram ⟹

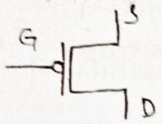


Layout:

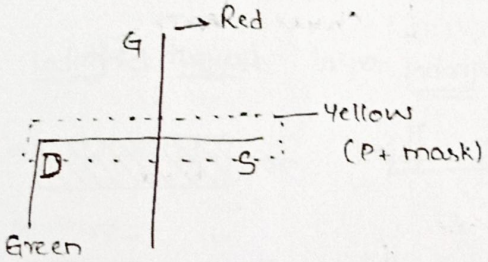


⟹ with dimensions

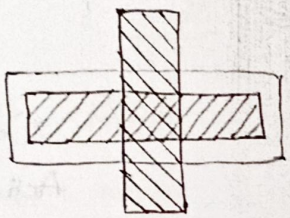
PMOS:



Stick diagram



Layout



03/08/18

CMOS Design:-

Stick diagram:

The connection material b/w diffussion and metal is called Contact.

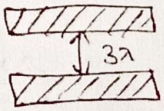
The connection material b/w metal and metal2 is called via.

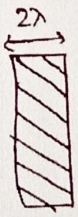
Layout Design Rules:

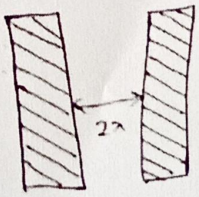
* The most used rules are λ-based design rules.
* Design rules are the Geometric dimensions.
* These rules helps the designer / Fabricate engineer to convert the stick diagram into layout to get the desired specifications of the device & circuit.
* These rules also helps for proper designing of layout (physical design) with dimensions.
* All the layout dimensions are represented with λ units.

$L = 2\lambda$ L = channel length.

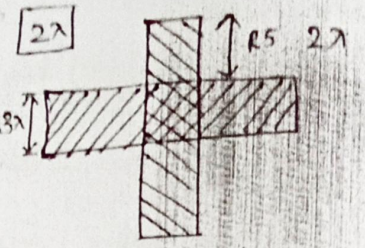
Rule No	Description	λ-Rule
	Active Area Rules	
R_1	Minimum active area width	3λ
R_2	Minimum active area spacing	3λ
	Poly Silicon Rules	
R_3	Minimum polysilicon width	2λ
R_4	Minimum poly spacing	2λ



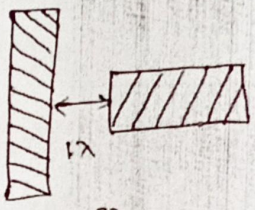




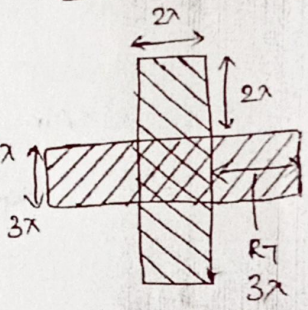
Rule No	Description: Active Area Rules	λ - Rule
R5	Minimum gate Extension of polysilicon over active area	2λ



R6	Minimum poly to active edge spacing (poly outside the active area).	1λ

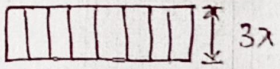


R7	Minimum poly to active edge spacing (poly inside the active area)	3λ

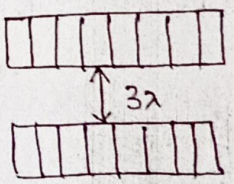


Metal Rules

R8	Minimum Metal Width	3λ

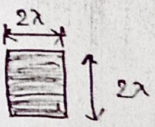


R9	Minimum Metal Spacing	3λ

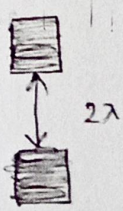


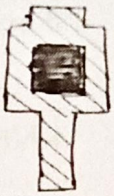
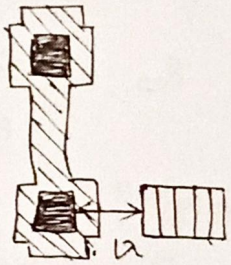
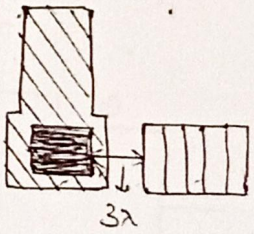
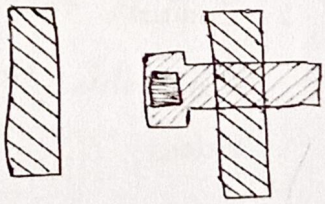
Contact rules

R10	Poly contact size	2λ



R11	Minimum poly contact Spacing	2λ

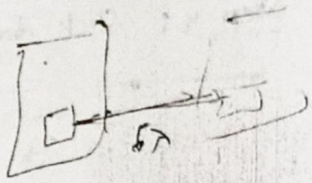


Rule No	Description	λ-Rule	
	Active Area Rules		
R12	Min poly contact to edge Spacing	1λ	
R13	Min poly contact to metal edge spacing	1λ	
R14	Min poly contact to active edge spacing	3λ	
	Active area Contact Rules		
R15	Active area contact size	2λ	
R16	Minimum active area contact Spacing (on same active region)	2λ	
R17	Minimum active contact to active edge spacing	1λ	

R18 Minimum active contact to metal edge spacing — 1λ

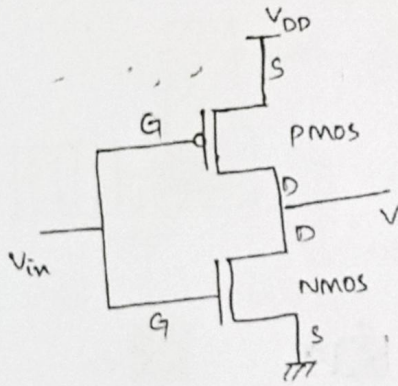
R19 Minimum active contact to poly edge spacing — 3λ

R20 Minimum active contact spacing (on diff active regions) — 6λ

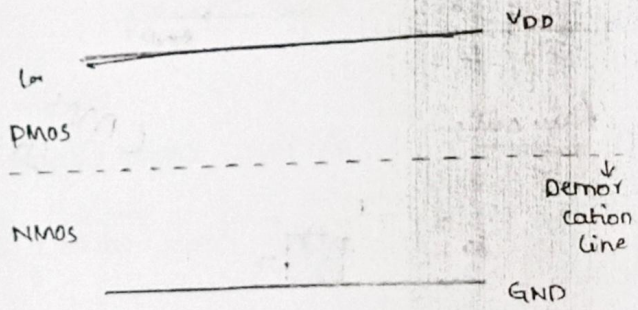


07/08/2018

Draw the layout of CMOS Inverter:



For drawing Stick diagram/layout, we need to follow following steps:



1. Draw power rails V_{DD}, GND
2. Indicate the demarcation line (To draw PMOS & NMOS)
   Above this line → PMOS
   Below " " → NMOS
3. Draw the Transistors (PMOS & NMOS)
4. Routing - Make the interconnections according to the circuit diagram.

Step 1

VDD

GND

Step 2

VDD

GND

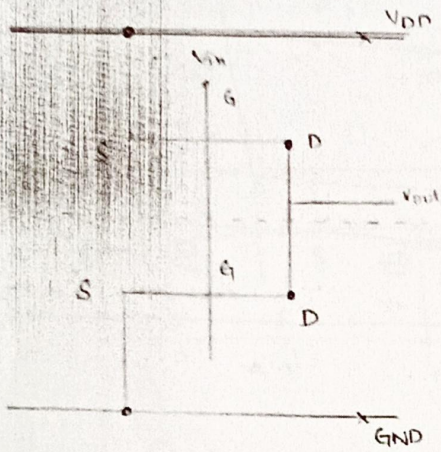
Step 3

G

S D

S G D

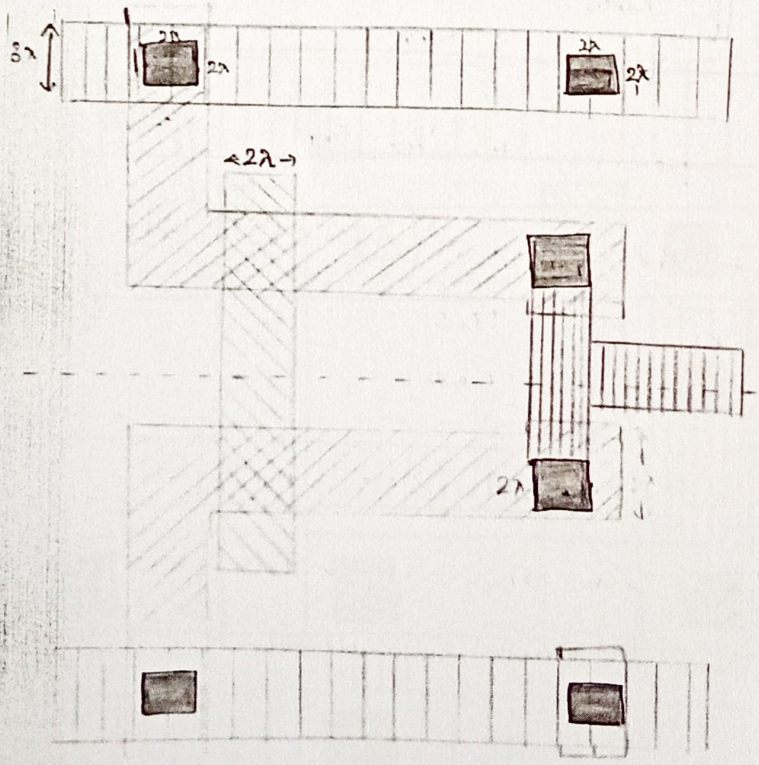
Step 4: Stick diagram



Layout:

Layout:

CMOS Inverter



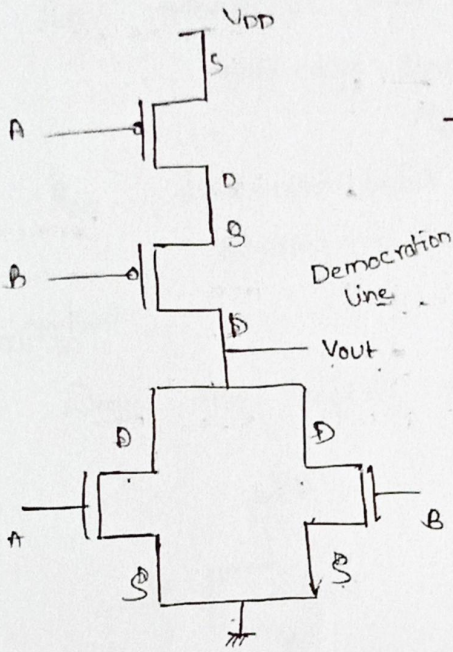
Pwell

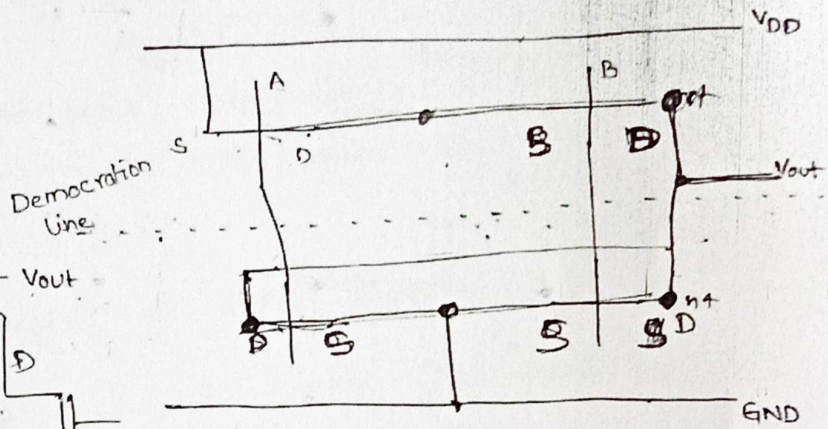
08/08/18

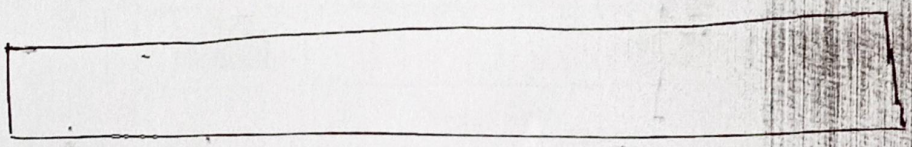
CMOS NOR GATE:

NOR GATE : $\overline{A+B}$

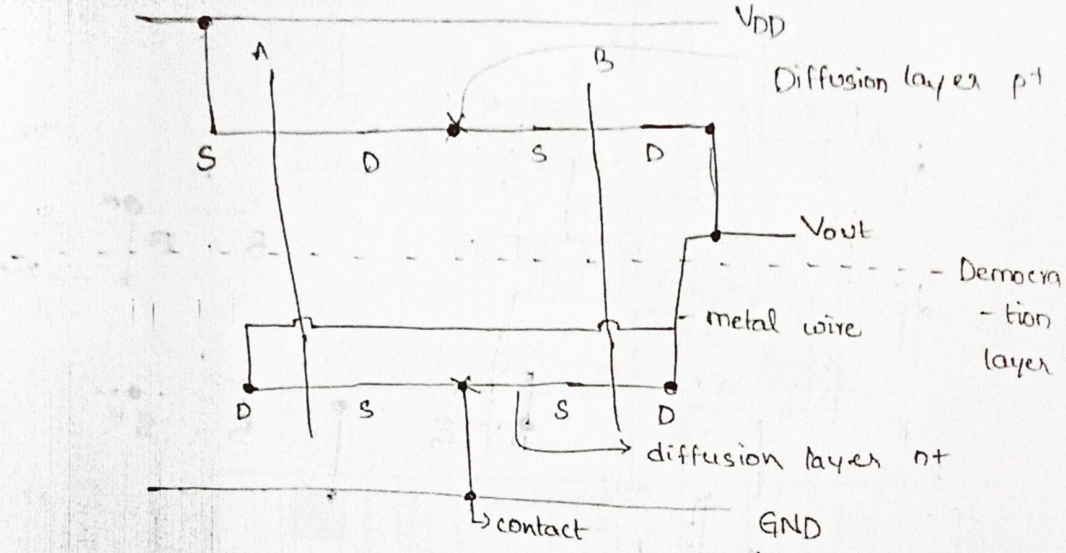
Stick diagram:



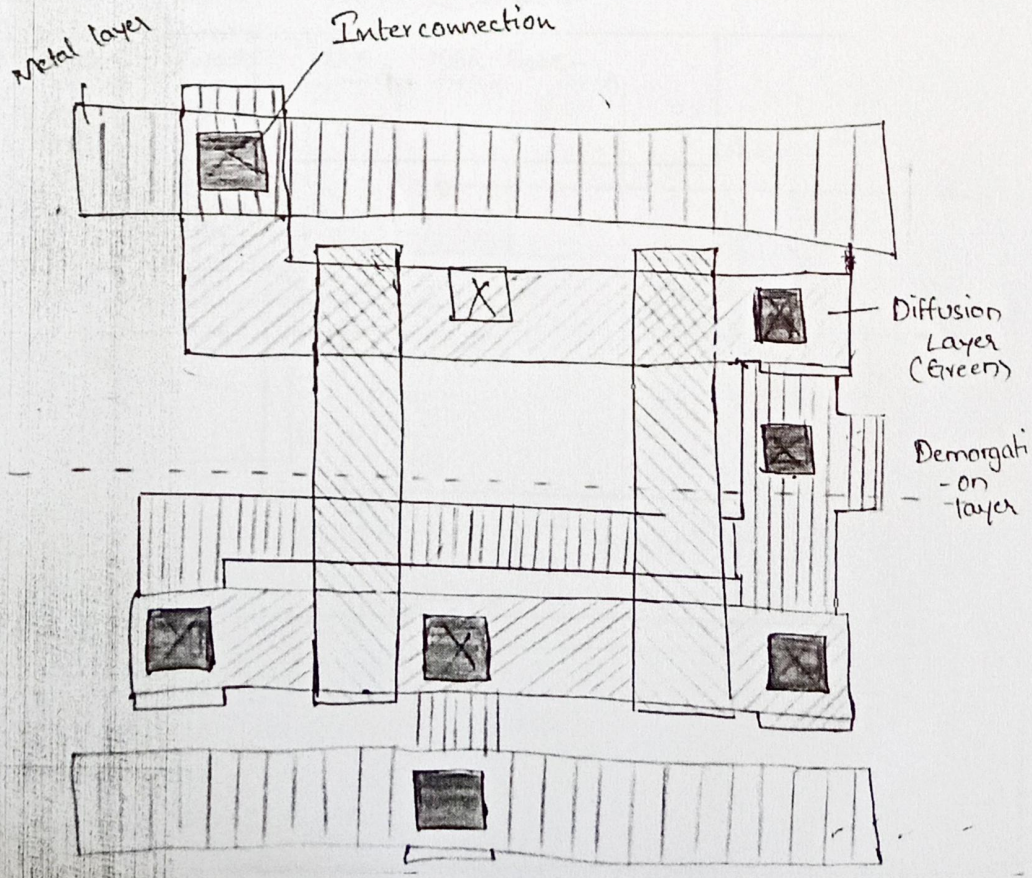




Stick diagram (NOR Gate)

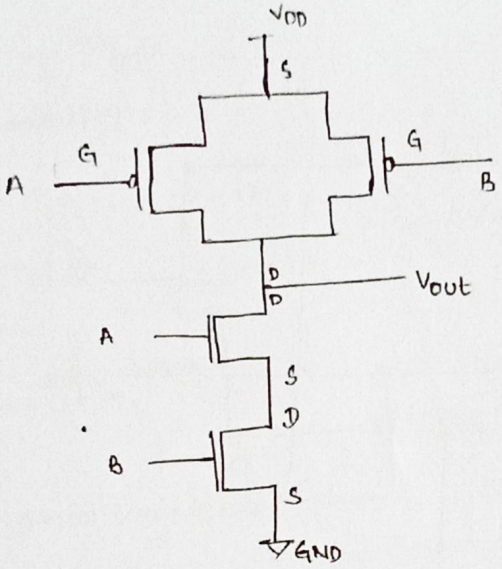


Layout Design:

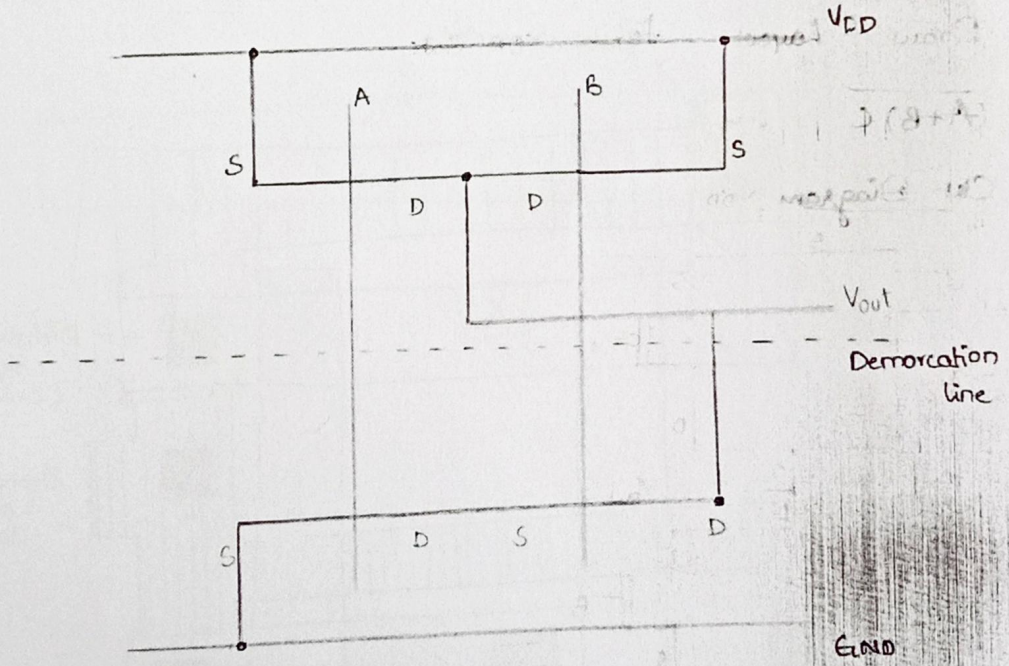


Draw the layout for the NAND Gate:

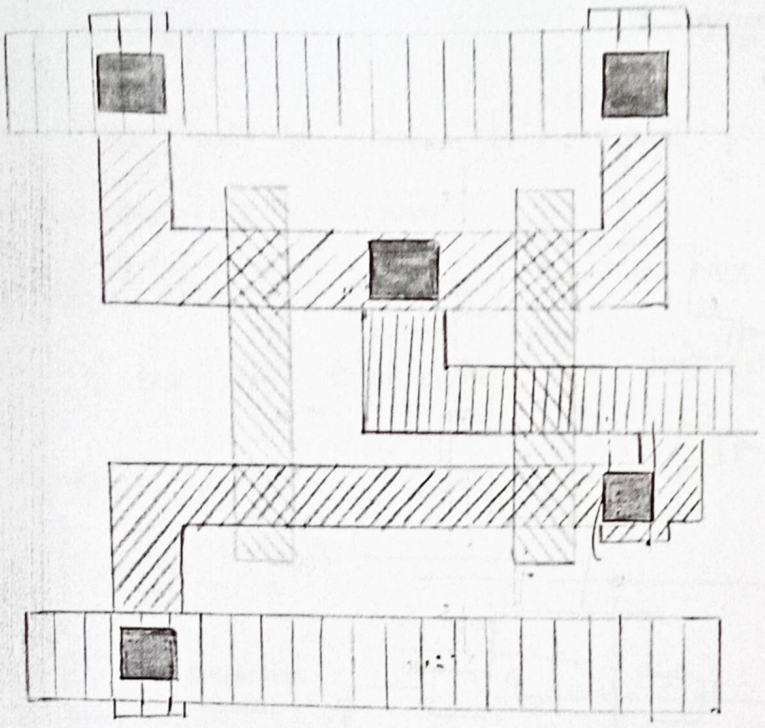
CKt Diagram:



Stick Diagram



NAND GATE: LAYOUT:

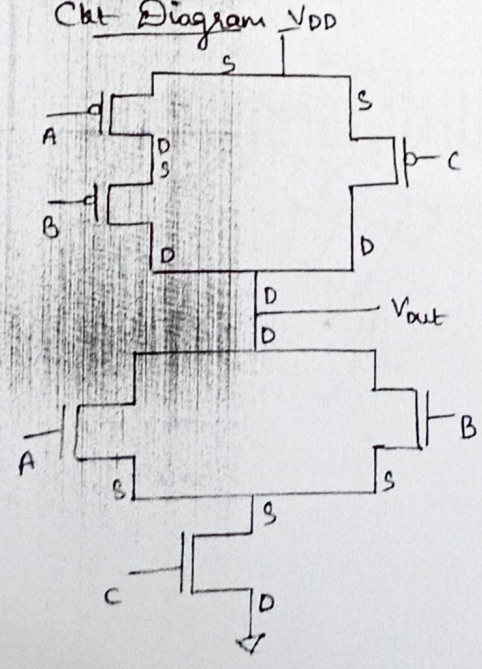


Draw Layout for $\overline{(A+B)C}$..

Draw Layout for XOR Gate-

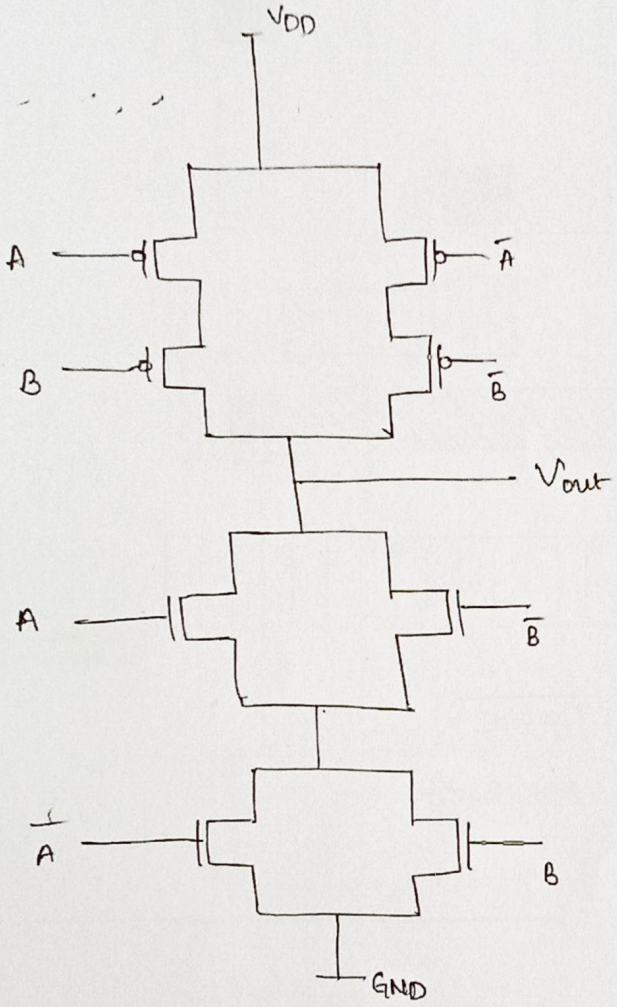
$\overline{(A+B)C}$

Ckt Diagram

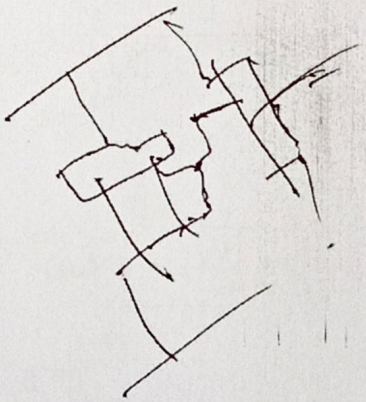


XOR Gate

Ckt Diagram



AB



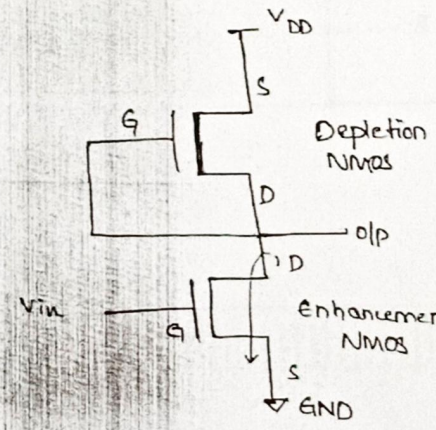
13/08/18

N-MOS Inverter

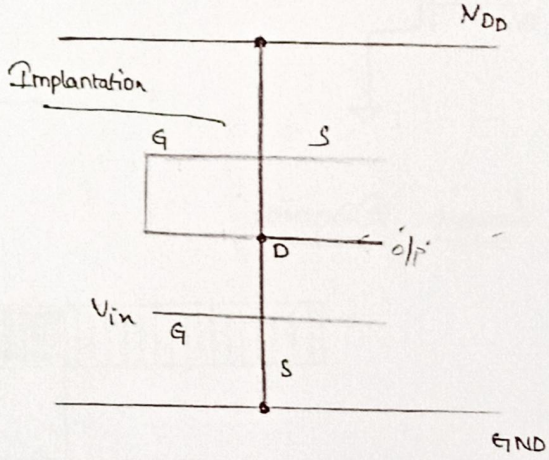
→ Driver ckt will be same (ie, NMOS part of the pull down ckt is same)

→ PMOS ckt is replaced by N-MOS depletion ckt (bcz for Enhancement, we don't get full swing)

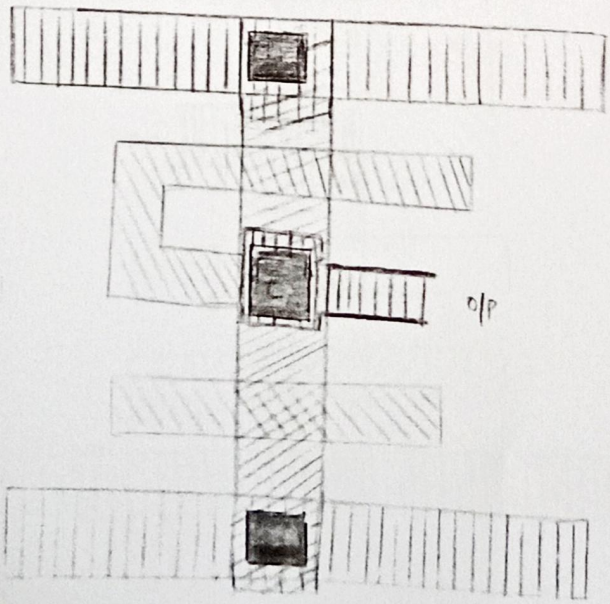
* Ckt diagram:



Stick diagram

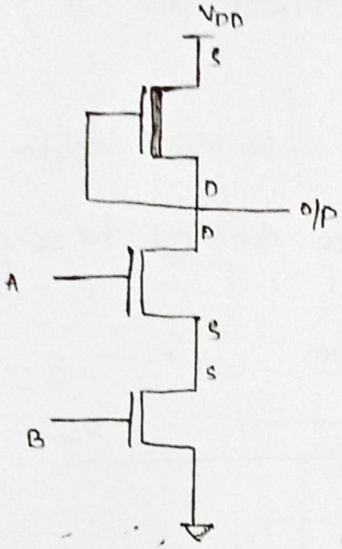


LAYOUT:

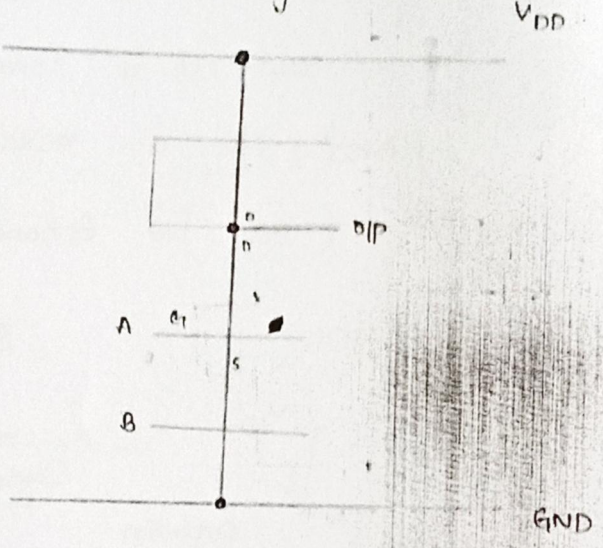


Draw Layout for NMOS NAND Gate:

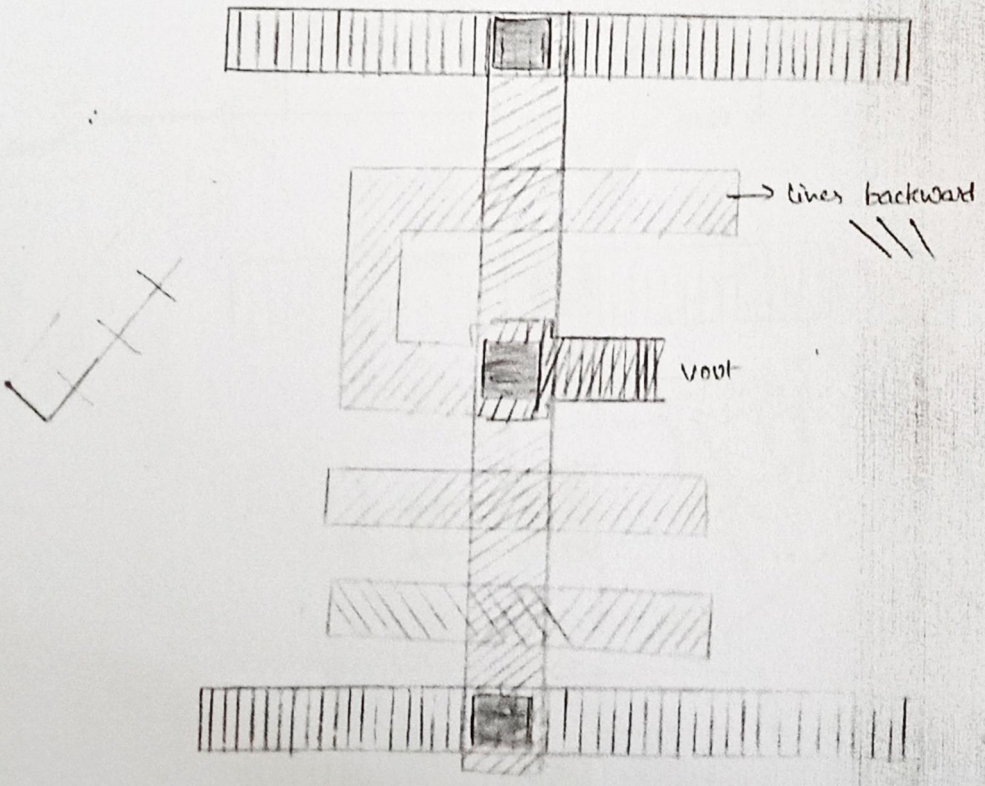
* All the PMOS Transistors are replaced by single depletion NMOS Transistor.



Stick diagram:



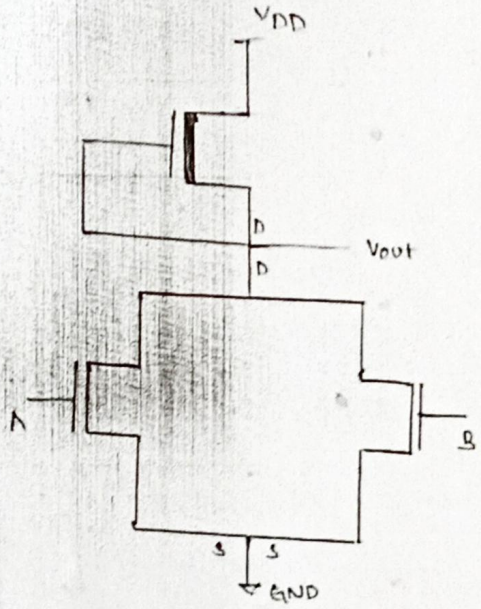
Layout Diagram:

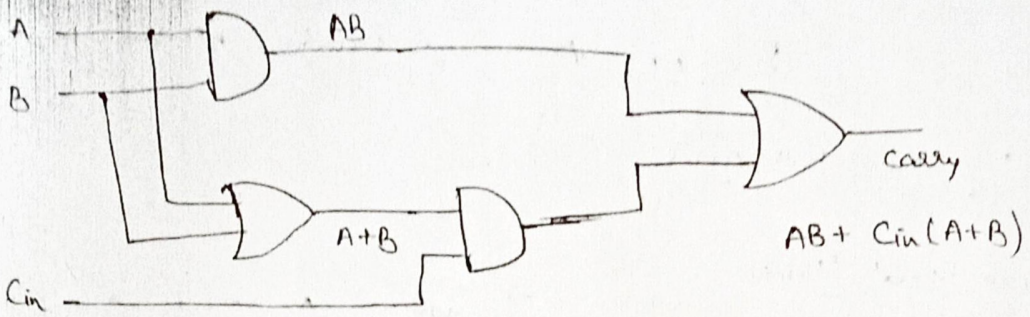


Draw layout for NMOS NOR Gate:

13

Circuit Diagram

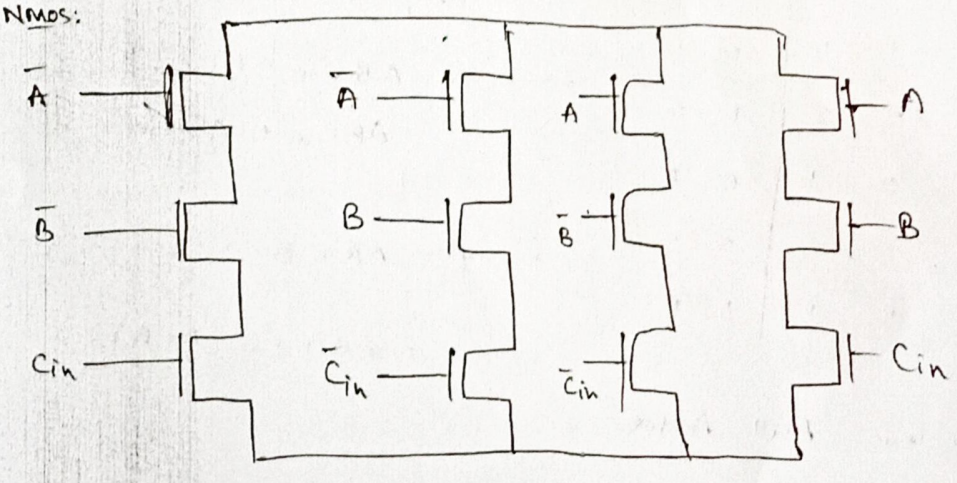




Transistor level diagram:

Sum: $\bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$

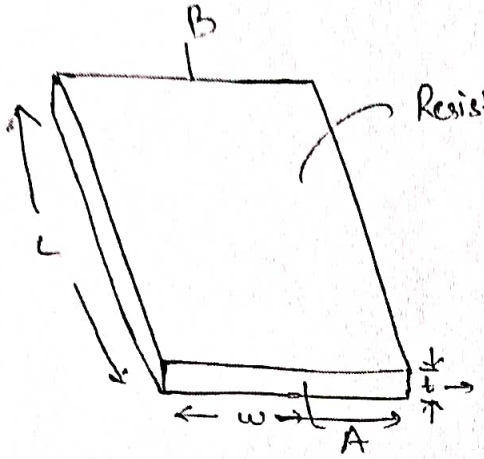
Nmos:



UNIT - IV

Basic Circuit Concepts

Sheet Resistance (R_S): Resistance of the square sheet b/w ends A & B (R_{AB})



Resistance,

$$R = \frac{\rho l}{A}$$

A - Cross-Section Area

A = Length x breadth = w x t

Sheet Resistance, $R_{AB} = \frac{\rho l}{A} = \frac{\rho l}{t \cdot w}$

For Square sheet, $l = w$

$$\Rightarrow \boxed{R_S = R_{AB} = \frac{\rho}{t}} \text{ ohms/square}$$

~~Resistivity depends on~~

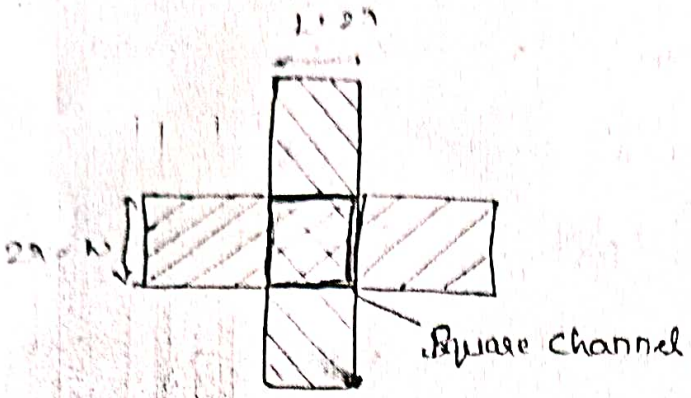
$\Longrightarrow$ Resistance of Sheet depends on 'Resistivity' of Sheet and thickness & but not on length & width of sheet/wire

For example, a 1 μm square sheet offering 10kΩ resistance, even if it is a 1cm square sheet offering the same resistance i.e., 10kΩ

Apply Sheet resistance concept to MOS Transistors:

Consider, $2\lambda \times 2\lambda$ — length, L - polysilicon

$\frac{1}{L}$ $\frac{1}{w}$ — w - diffusion layer



'Z' - Length to width ratio of channel.

$Z = \frac{L}{W}$

Total Resistance, $R = Z \cdot R_s$

R_s - unit Square sheet Resistance

$= \frac{2\lambda}{2\lambda} \cdot R_s$

$= R_s$

$= 10^4 \times 1\ \Omega$ — typical R_s for 5μm Technology

$R = 10K\Omega$

Typical values of Sheet Resistance R_s for 5μm Technology, 2μm Tech. & 1.2μm Tech.

Layer	ohms per square & Sheet Resistance 5μm	2μm	1.2μm
1. Metal	0.03	0.04	0.04
2. Polysilicon	15 - 100	15 - 30	15 - 30
3. Diffusion / Active layer	10 - 50	20 - 45	20 - 45
4. N transistor channel	10^4	2×10^4	2×10^4
5. P transistor channel	2.5×10^4	4.5×10^4 approx	4.5×10^4
6. Silicides	2 - 4	— (negligible)	—

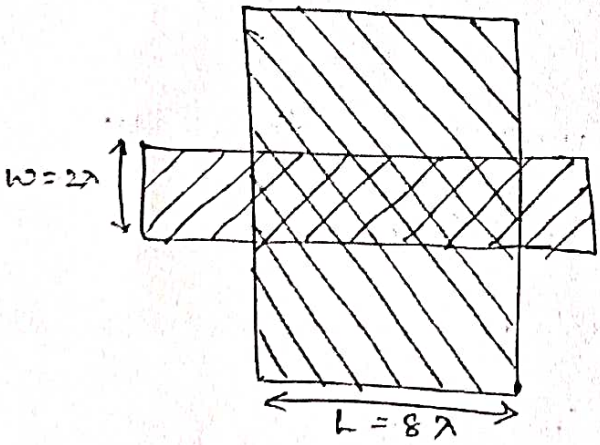
Silicides: Silicides are the low resistive material which are used in high speed applications.

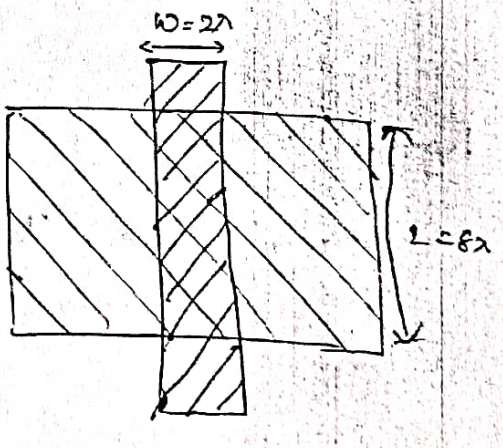
→ Silicides are designing / preparing (-ed) (-an) by depositing the metal layer on polysilicon. This process is called evaporation process / sputtering

Calculate resistance of NMOS Transistor considering the Z is 4:1 ratio.

Sol: $Z = 4:1 \Rightarrow L = 4x, \quad W = 1x$

Let the dimensions be $8\lambda \times 2\lambda$





$$R = Z \cdot R_s = 4 \times 10^4$$

$$= 40K\Omega.$$

$\left\langle Z = \frac{8}{2} = 4 \right\rangle$

Consider a p-transistor, then $R = Z \cdot R_s$

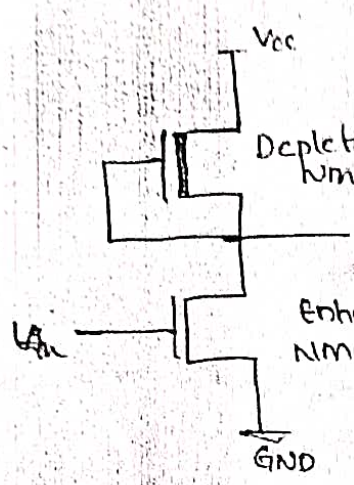
$$= 4 \times 2.5 \times 10^4$$

$$= 10 \times 10^4$$

$$= 100K\Omega$$

Apply Sheet Resistance concept to Inverters.

NMOS Inverter:-



→ Pull Up Transistor

→ Pull Down Transistor.

$$Z_{PU} = \frac{L_{PU}}{W_{PU}}$$

$$Z_{P-D} = \frac{L_{PD}}{W_{PD}}$$

Pull up to Pull down ratio,

$$\frac{Z_{PU}}{Z_{PD}} = \frac{4}{1} \quad \text{(for NMOS)}$$

$$\Rightarrow Z_{PU} = \frac{4}{1} \rightarrow 4:1$$

$$Z_{PD} = \frac{1}{1} \rightarrow 1:1$$

∴ ON Resistance of PU Transistor, $R_{ON} = ZR_s = 4 \times 10^4$

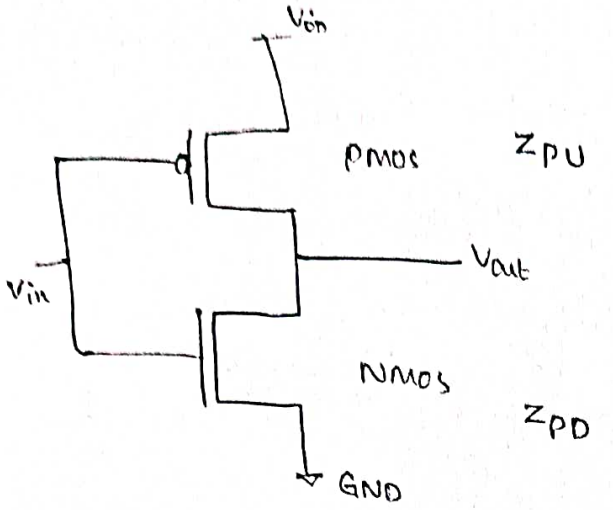
$= 40\,k\Omega$

ON Resistance of PD Trans, $R_{ON} = ZR_s = 1 \times 10^4$

$= 10\,k\Omega$

Total $R_{ON} = 40\,k\Omega + 10\,k\Omega = \underline{50\,k\Omega}$

For CMOS Inverter:



Pull up to Pull Down Ratio,

$$\frac{Z_{PU}}{Z_{PD}} = 1:1$$

$$\Rightarrow Z_{PU} = 1:1$$

$$Z_{PD} = 1:1$$

PMOS $R_{ON} = ZR_S = 1 \times 2.5 \times 10^4$

$= 25\ K\Omega$

NMOS $R_{ON} = ZR_S = 1 \times 10^4$

$= 10\ K\Omega$

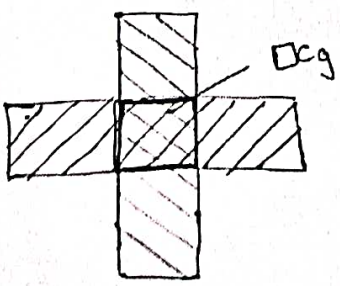
This concept can't be applicable for all CMOS circuits. It can only be applied to NMOS circuits.

Capacitance:

$$\text{Capacitance, } C = \frac{\varepsilon_{ins}\,\varepsilon_0\,A}{D}$$

Square C_g $\square C_g$ – Standard Gate Capacitance.

This stand. Gate Capacitance are considered when length and width are same ($L = W$) feature size



Diff metal layers: metal 1 – 12 ↓ highest thickness Used for routing high power rails

Typical Capacitance values for NMOS Circuit:

No layers Capacitance	capacitance value in $pf \times 10^{-4}/\mu m^2$ (Relative values)		
	5 μm	2 μm	1.2 μm
1. Gate to Channel Capacitance	4 (1)	8 (1)	16 (1)
2. Diffusion Capacitance	1 (0.25)	1.75 (0.22)	3.75 (0.23)
3. Polysilicon to Substrate	0.4 (0.1)	0.6 (0.075)	0.6 (0.038)
4. Metal 1 to Substrate	0.3 (0.075)	0.33 (0.04)	0.33 (0.02)
5. Metal 2 to Substrate	0.2 (0.05)	0.17 (0.02)	0.17 (0.01)
6. Metal 2 to Metal 1	0.4 (0.1)	0.5 (0.06)	0.5 (0.03)
7. Metal 2 to polysilicon	0.3 (0.75)	0.3 (0.028)	0.3 (0.018)

$$\text{Relative value} = \frac{\text{Specified value}}{\text{Gate to Channel Capacitance value}}$$

Standard Gate Capacitance for different Technology:

For 5μm Technology: Standard Capacitance value for 5μm Technology is given by

$$\square C_g = \text{area} \times \text{Capacitance value}$$

$$= \underbrace{5\,\mu m * 5\,\mu m}_{25\,\mu m^2} * 4 \times 10^{-4}\ pf/\mu m^2$$

$$\square C_g = 0.01 pf.$$

for 2 um technology

:standard gate Capacitance value $\square C_g$-

→ area of Capacitance layers * Capacitance valu

= 2um x 2um x 8×10^{-4}

→ 0.0032pf.

-for 1.2um technology :-

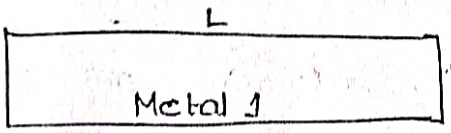
= area * Capacitance value.

→ 2um x 2um x 16×10^{-4}

⇒ 0.0023pf.

Capacitance values for different layers :-

Metal1 layer :-



Length = 20λ

width = 3λ.

⇒ 20λ x 3λ

* Calculate the Capacitance value in terms of $\square C_g$ units?

Sol: Relative Area :-

It is ratio between the area of specified layer and area of standard gate (Square gate).

$$= \frac{20\lambda \times 3\lambda}{2\lambda \times 2\lambda} = 15\lambda$$

Capacitance value = Relative area * Relative Capacitance value

* -for 5 um technology, Calculate C. value?

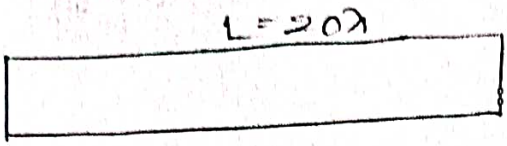
= Relative area * Relative Capacitance value. $\square C_g$.

= 15 x 0.075 $\square C_g$

→ 1.125 $\square C_g$.

The defined area in metal has a capacitance in Subs. triple 1.52 times that of feature size square gate area. Similarly

Polysilicon :-



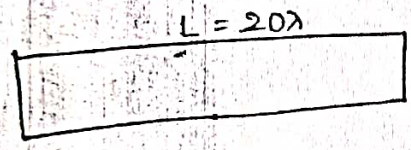
. Calculate capacitance in terms of Square C_g ?

$$\text{Relative area} = \frac{20\lambda \times 3\lambda}{2\lambda \times 2\lambda} = 15.$$

For 5um, Capacitance = Relative area * Relative Capacitance

$$= 15 \times 0.1 = 1.5\ \square C_g.$$

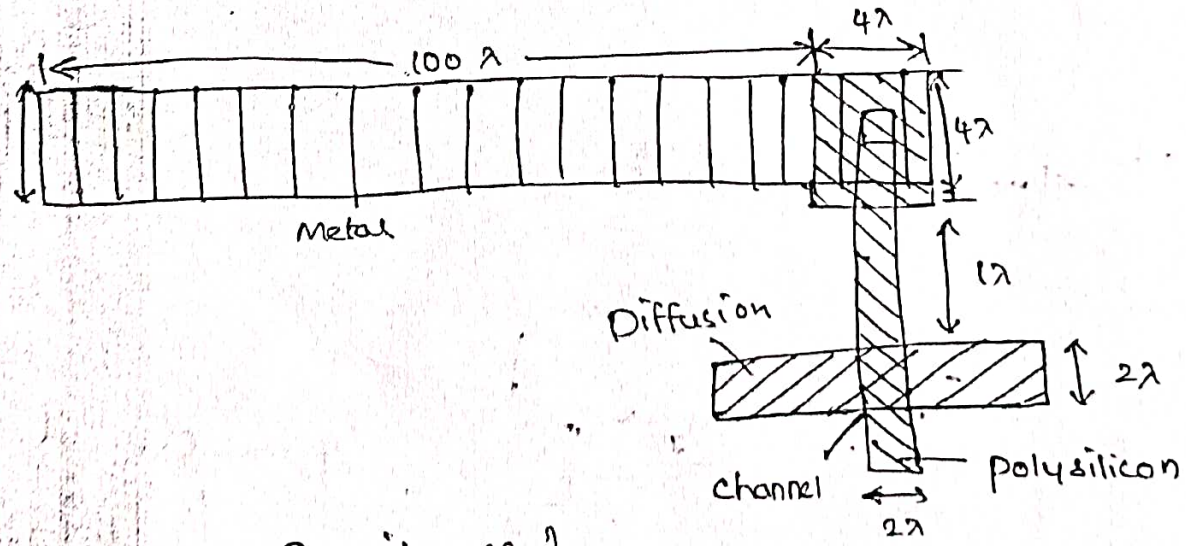
for Diffusion :-



for 5um, Capacitance = Relative area * Capacitance value

$$= 15 \times 0.25 = 3.75.$$

* Multiple Layers:



Calculate the Capacitance !

(1) For Metal1: $L = 100\lambda$, $W = 3\lambda$

$$\text{Relative Area} = \frac{100\lambda \times 3\lambda}{2\lambda \times 2\lambda} = 75$$

For 5 Micron Tech:

Capacitance = Relative Area × Relative Capacitance

= 75 × 0.075 □Cg

= 5.625 □Cg

② For Poly Silicon: (Exclude Gate Region)

Relative Area = (4λ × 4λ) + (3λ × 2λ)

$= \frac{22\lambda^2}{4\lambda}$ $\left\langle \because \frac{22\lambda}{2\lambda \times 2\lambda} \right\rangle$

Capacitance = $\frac{22\lambda}{4\lambda}$ × 0.1 □Cg

= 0.55 □Cg

5.625
0.55
6.175

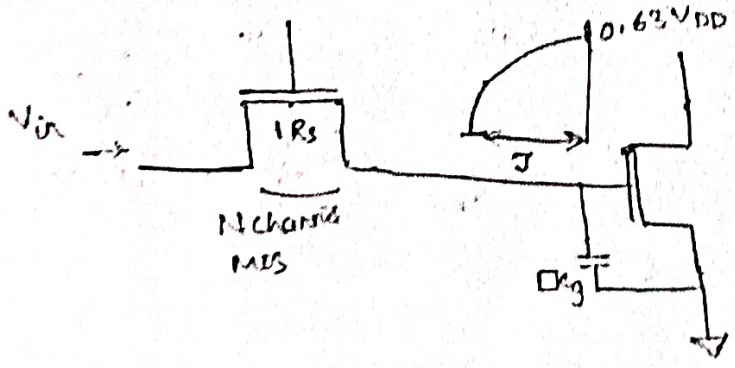
③ Gate Capacitance = 1 □Cg (C_g)

~~Relative~~ Total Capacitance, $C_T = C_M + C_P + C_g$

= (5.625 + 0.55 + 1) □Cg

= 7.175 □Cg

Delay Time (τ):



Square channel

↓

10^4 - 10KΩ R

Delay Time τ is defined as one Standard Gate Capacitance ($1\,\square C_g$) is charging through one N□Channel NMOS pass Transistor ($1\,R_s$)

$$\Rightarrow \quad \tau = 1R_s \times 1\,\square C_g \text{ sec}$$

for 5μm Technology:

Time delay, $\tau = R_s \times \square C_g$ sec

$= 10^4 \times 0.01$ pf

$= 0.1$ n sec

for 2μm Technology,

Time delay, $\tau = R_s \times \square C_g$

$= 2 \times 10^4 \times 0.0032$ pf

$= 0.032$ n sec $\times 2 = 0.064$ n sec

for 1.2μm Technology,

Time delay, $\tau = R_s \times \square C_g$

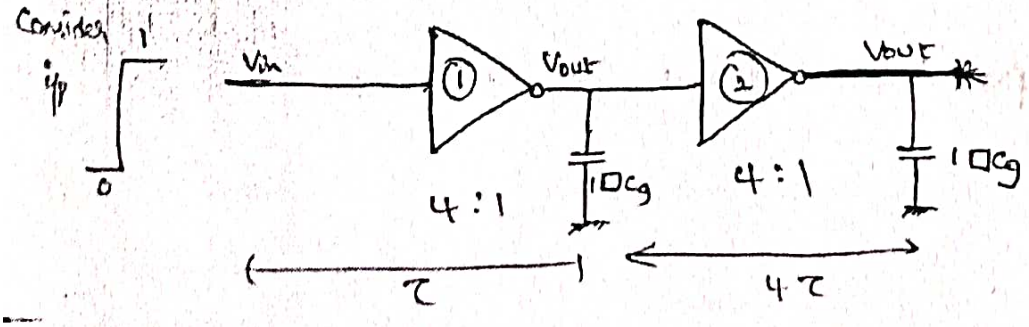
$= 10^4 \times 2 \times 0.0023$ pf

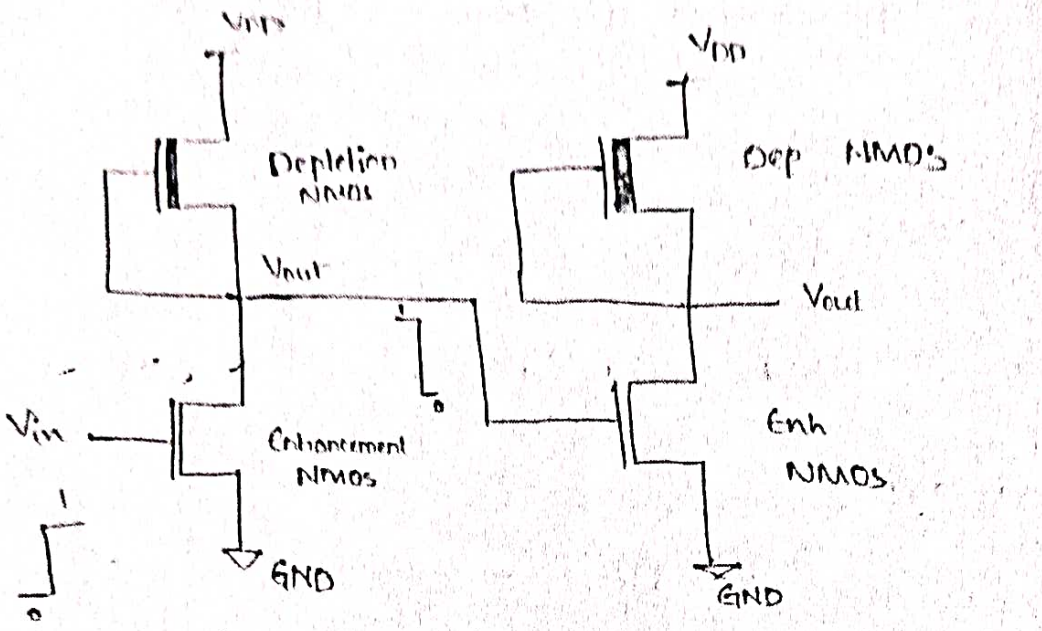
$= 0.046$ n sec

11/09/18

Inverter Delays:

Cascading NMOS Inverters:





Delay Time (τ):

$$\text{Delay Time, } \tau = R_s \times \square C_g$$

First Inverter, pull down Transistor is considered

$$\Rightarrow R_s = 10^4 = 10K\Omega$$

For 2nd Inverter, pull up transistor is considered,

$$R_s = 40K\Omega$$

$$\therefore \text{Total Delay Time} = \overbrace{(1R_s \times 1\square C_g)}^{\text{Pull Down}} + \overbrace{(4R_s \times 1\square C_g)}^{\text{pull up}}$$

$$= 1\tau + 4\tau$$

$$= 5\tau$$

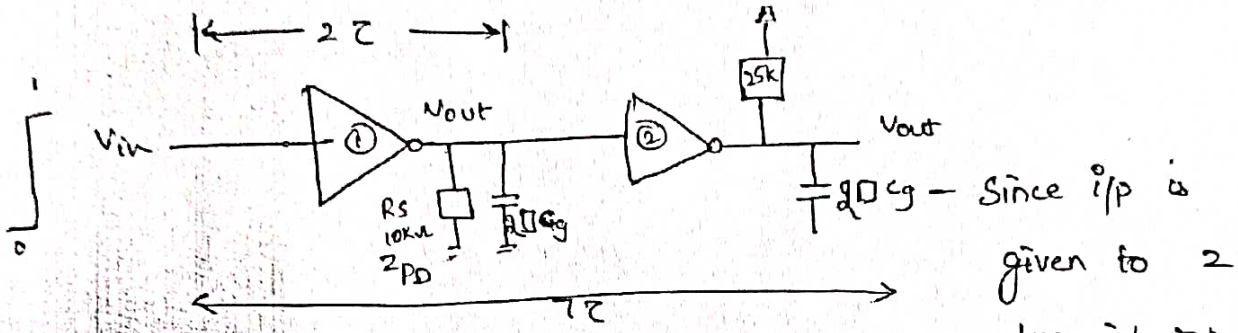
If ratio is 8:1 $\Rightarrow$ Delay time $= 9\tau$ $(1\tau + 8\tau)$

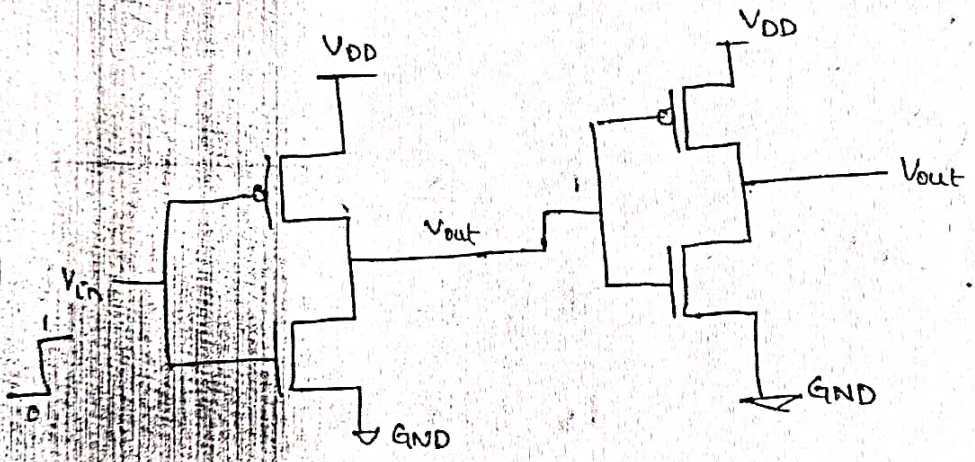
pull down always < pull up

For NMOS Inverters, Delay = $\left(1 + \frac{Z_{PU}}{Z_{PD}}\right)\tau$

Ex: For $\frac{Z_{PU}}{Z_{PD}} = 4:1 \Rightarrow$ Delay = 5τ

CMOS Inverters:





Delay Time:

For First Inverter, pull down is considered, & $R_S = 10K\Omega$

Delay Time = $1R_S \times 2\square C_g$

$= 2\tau$

For 2nd Inverter, pull up is considered, $R_S = 25K\Omega$

Delay Time = $2.5R_S \times 2\square C_g$

$= 5\tau$

Total Delay Time = 7τ

The amount of charge that moves into the plates depends upon the capacitance and the applied voltage

$Q = CV$

Q – charge in coulombs

C – capacitance in farads

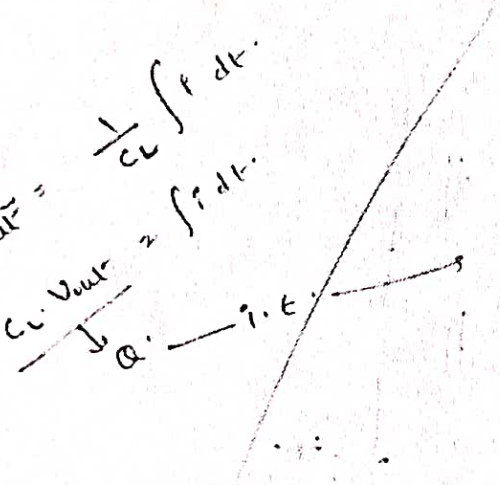
V – potential difference b/w plates in volts.

$C = \frac{Q}{V}$

Capacitance

$V_{out} = \frac{1}{C} \int i\,dt$

$C.V_{out} = \int i\,dt$



$I = \frac{Q}{t}$

$Q = It$

$dQ = I\,dt$

Total charge $\int dQ = \int I\,dt$ (constant)

$Q = I \int dt$

Charge proportional to applied voltage.

$Q = CV$

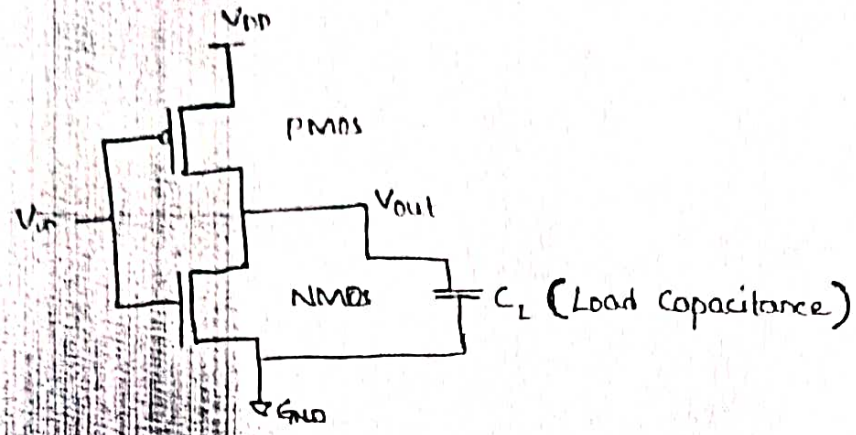
$V = \frac{Q}{C}$

$$V = \frac{1}{C} \int I\,dt$$

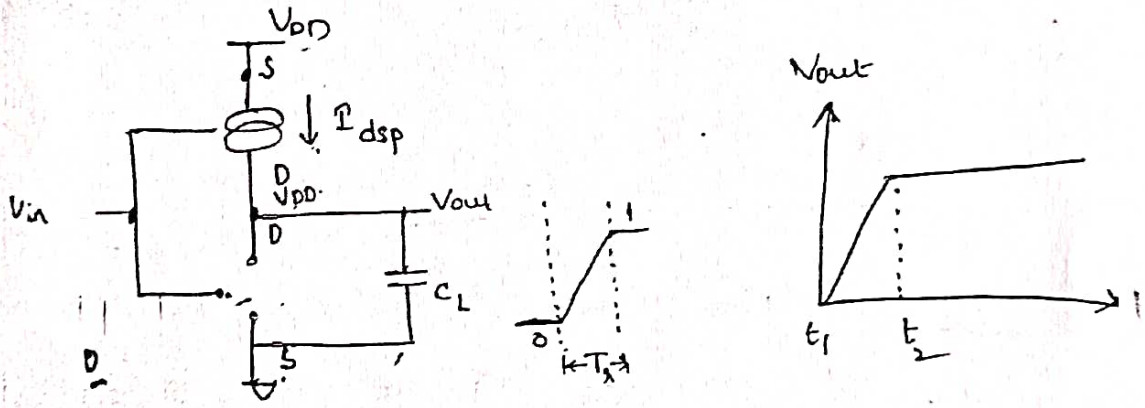
o/p voltage across capacitor when current changes with respect to time.

Unit-1

Calculation of CMOS Inverter Delays:



Rise Time (T_R): Time taken to change the output of CMOS Inverter from logic '0' to logic '1'.



op voltage, $V_{out} = \frac{1}{C_L} \int I_{dsp}\, dt$

$= \frac{1}{C_L} \cdot I_{dsp} \cdot t$

$\Rightarrow t = \frac{V_{out} \cdot C_L}{I_{dsp}}$ .0

But Saturation current for PMOS,

$I_{dsp} = \frac{\beta_p}{2} (V_{gs} - V_t)^2$

$$\Rightarrow t = \frac{2 V_{out} \cdot C_L}{\beta_p (V_{gs} - V_t)^2}$$

$$V_{gs} - V_g - V_s = V_{DD}$$

$$V_t = 0.2 V_{DD}$$

V_{out} = max. level = V_{DD}

$$\therefore t = \frac{2 V_{DD} \cdot C_L}{\beta_p (V_{DD} - 0.2 V_{DD})^2} = \frac{2 V_{DD} \cdot C_L}{\beta_p (0.8\ V_{DD})^2}$$

$$t = \frac{2 C_L}{\beta_p (0.8)^2 V_{DD}}$$

$(0.8)^2 = 0.64$

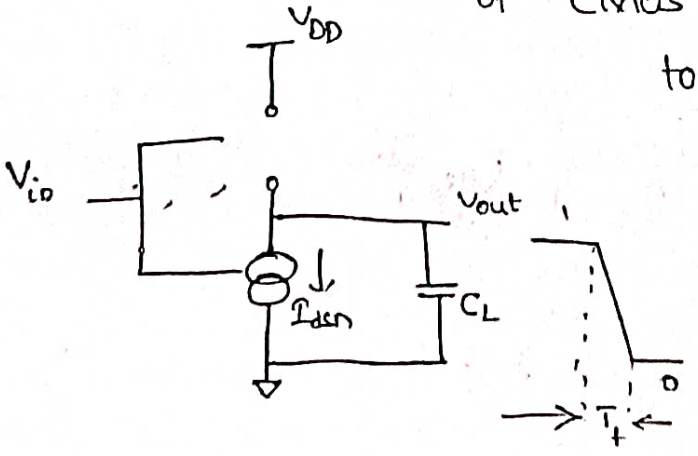
$= 2/0.64$

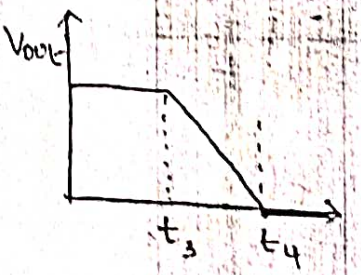
$= 3.125$

$\tau_r = t_2 - t_1$

$$\therefore \boxed{t = T_r = \frac{3 C_L}{\beta_p V_{DD}}}$$

<u>Fall time</u> :- Time taken to change the output of CMOS Inverter from logic '1' to logic '0' is called "Fall time".





⇒ 1. At t_3, $V_{out} = 1$

At t_4, $V_{out} = 0$

$$\Rightarrow V_{out} = \frac{1}{C_L} \int I_{dsn}\, dt = \frac{1}{C_L} \cdot I_{dsn} \cdot t$$

$$t_f = \frac{V_{out} \cdot C_L}{I_{dsn}}$$

$$I_{dsn} = \frac{\beta_n}{2}(V_{gs} - V_t)^2$$

$$\Rightarrow t_f = \frac{2 \cdot V_{out} \cdot C_L}{\beta_p (V_{gs} - V_t)^2}$$

$$\Rightarrow t_f = \frac{2 \cdot V_{DD} \cdot C_L}{\beta_p (0.8\, V_{DD})^2}$$

$V_{gs} = V_{DD}$

$V_t = 0.2\, V_{DD}$

$V_{out} = V_{DD}$

$t_f = t_3 - t_4$

$$\text{Fall time, } T_f = \frac{3C_L}{\beta_p V_{DD}}$$

From the expressions Rise time & Fall time,

→ T_r & T_f are proportional to Load Capacitance

→ T_r & T_f are inversely proportional to V_{DD}

$$\mu_p = 2.5\mu_n$$

$$\left(\frac{W}{L}\right)_p = 2.5 \left(\frac{W}{L}\right)_n$$

$$\beta_p = 2.5\, \beta_n$$

Then, we get $T_r = T_f$

If both dimensions are equal then Rise time would be more than that of fall time by 2.5 times (Since mobility is high in NMOS)

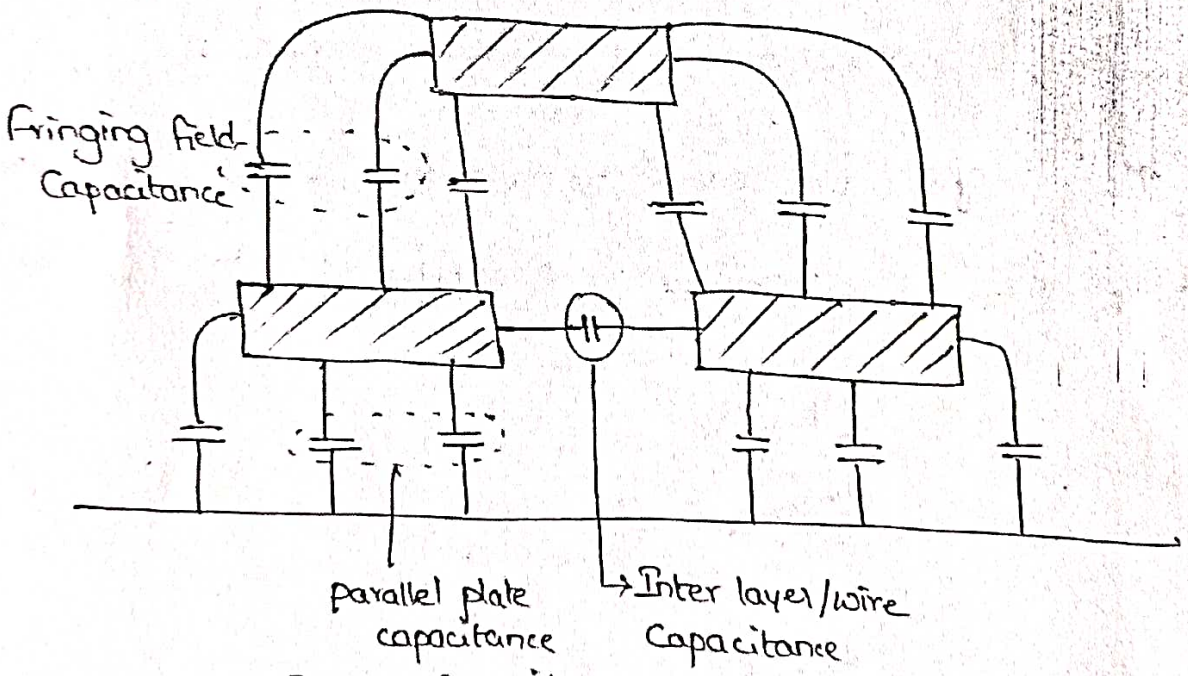
$$T_r = 2.5\, T_f$$

Wiring Capacitance

Capacitance due to different layers w.r.t Substrate is known as wiring capacitance / parasitic capacitance.

It is of 3 types:

1. Fringing field capacitance
2. Inter layer "
3. Peripheral "



1. Fringing field Capacitance:

Capacitance formed due to fringing field is called fringing field Capacitance.

→ Higher composed to other

Interlayer Capacitance:

Capacitance formed from one layer to another layer may be b/w metal layers / metal to substrate

Peripheral Capacitance

Peripheral Capacitance is formed due to the peripheral devices (which are formed in P-well / N-well proces) peripheral device to substrate / wall.
side

Choice of Layers:

* Metal layers
* poly silicon layer
* Diffusion layer
* Silicides

UNIT – V

Short Channel Effects.

Scaling theory:

The slope of I_d on a logarithmic scale equals to

$$\frac{\partial(\log_{10} I_D)}{\partial V_{GS}} = (\log_{10} e)\frac{1}{nV_T}$$

the inverse of the above quantity is usually called the "subthreshold slope":

$$S = 2.3V_T\left(1+\frac{C_d}{C_{ox}}\right) \text{ V/dec}$$

* An emprical equation modelling of DIBL effect is

$$\mu_{eff} = \frac{\mu_0}{1+\theta(V_{GS}-V_{th})}$$

μ_0 – low field mobility

θ – fitting factor which is app Equals to $(10^{-7}/t_{ox})V^{-1}$

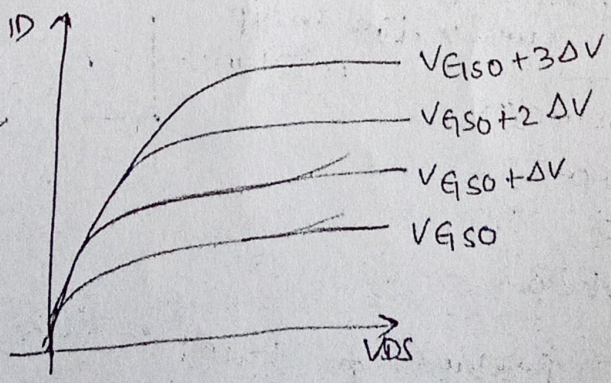
if $t_{ox} = 100$ A then $\theta = 1V^{-1}$ & mobility Exceeds 100mv.

$$I_D \approx \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}\left[1-\theta(V_{GS}-V_{TH})\right](V_{GS}-V_{TH})^2$$

$$\approx \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}\left[(V_{GS}-V_{TH})^2-\theta(V_{GS}-V_{TH})^3\right]$$

Velocity Saturation:-

$$I_D = V_{sat}\Theta_{id}$$
$$= v_{sat} W C_{ox}(V_{GS}-V_{th})$$



Effect of velocity saturation on drain current characterstics

Hot carrier Effects:-

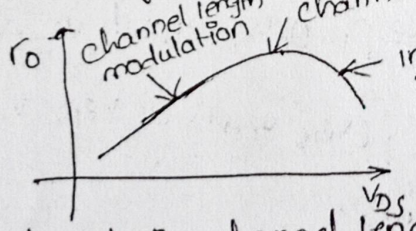
Hot carriers:- when the supply potential at the drain terminal is very large. The carriers will have the more velocity when compared to the previous state. These carriers are called Hot carriers.

Output impedance with drain to Source voltage we have 4 diag with V_{DS}, $V_{DS_1}+\Delta V$, V_{DS_2}, $V_{DS_2}+\Delta V$ and drain the characterstics also b/w V_{DS} & I_D with above supply voltage & o/p resistance r_o is given as

$$r_o = \frac{2L}{1-\frac{\Delta L}{L}} \frac{1}{I_D} \sqrt{\frac{qN_B}{2\epsilon_{Si}} (V_{DS}-V_{DS.sat})}$$

$V_{DS.sat}$ is the drain to Source voltage at pinchoff state

Graph b/w V_{DS} & r_o is given as

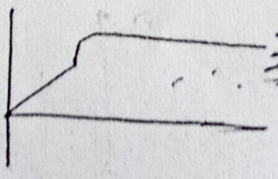


Mos device Models:-

level 1 → CL = 4μm (disadv is channel length is more)

level 2 → CL = >4μm [3.9 to 3.95] → get Drain 1) kink in curr
2) mobility is degraded

level 3 → CL = 1μm → kink in o/p resistance



BSim - 50 parameters
BSim-2 → 70 "
BSim-3 → 180 "
HSPICE - level 28.

An intresting feature of BSIM is the addition of a simple Equation to represent the geometry dependence

of many of the device parameters. the general expression is of the form

$$P = P_0 + \frac{\alpha_P}{L_{eff}} + \frac{\beta_P}{W_{eff}}$$

P_0 is the value of parameter for a long, wide transistor

($P = P_0$ if L_{eff}, W_{eff}, ∞)

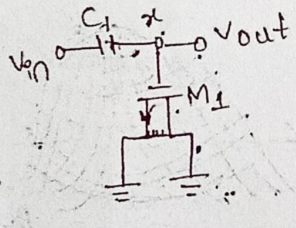
α_P & β_P are fitting factors

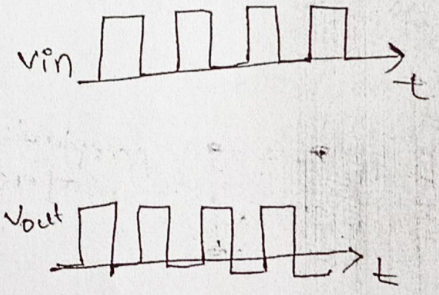
$$\mu = \mu_0 + \frac{\alpha_\mu}{L_{eff}} + \frac{\beta_\mu}{W_{eff}}$$

Other models

$$P = P_0 + \alpha\left(\frac{1}{L} - \frac{1}{L_{ref}}\right) + \beta\left(\frac{1}{W} - \frac{1}{W_{ref}}\right) + \left(\frac{1}{L} - \frac{1}{L_{ref}}\right)\left(\frac{1}{W} - \frac{1}{W_{ref}}\right)$$

Charge & capacitive Modelling :-





Triode region is also called as ohmic (or) linear region and in Saturation region

$C_{GS} = C_{GD} = (1/2) WL C_{ox} + WC_{ov}$

$C_{GS} = (2/3) WL C_{ox} + WC_{ov}$

Temp dependence :- Generally we have 2 types of temp dependance factors 1. +ve temp coefficient factor

2. -ve temp coefficient factor

+ve temp coeff factors are will increase with the temp

increment.

-ve temp coeff will decrease with the decrease temp

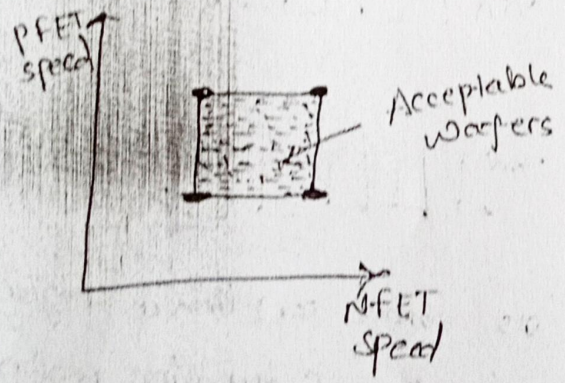
The temp dependence factor for MOSFET are V_{th}, built in potential of source & drain functions, the intrensic carrier concentration of silicon (n_i), the band gap energy (E_g) and the Mobility.

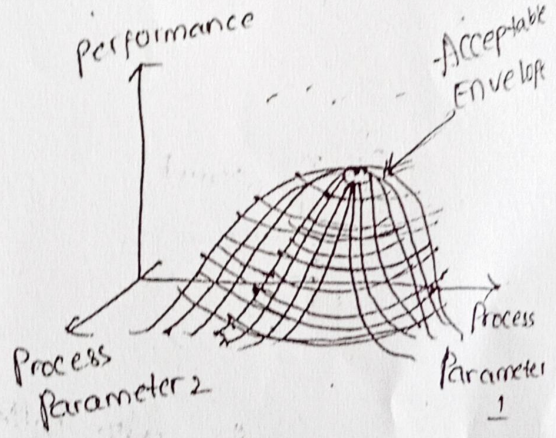
$$E_g = 1.16 - \frac{7.02 \times 10^{-4} T^2}{T + 1108}$$

$$\therefore \mu = \mu_0 \left(\frac{300}{T}\right)^{3/2}$$

Note: where $\mu_0 = \mu(T = 300^\circ K)$

Temp units are consider as either kelvin (or) °c dont use as °K.





The process corners are 4

1) fast NFET & fast PFET
2) Slow " " slow "
3) " " & fast "
4) fast " & slow "

Analog Design in a Digital World :-

V- Very high speed integrated ckt

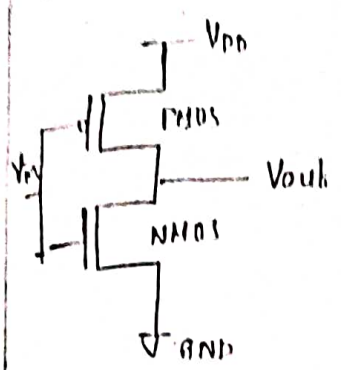
HH- hardware description language

V- very high speed integrated circuits.

In Hardware Description language.

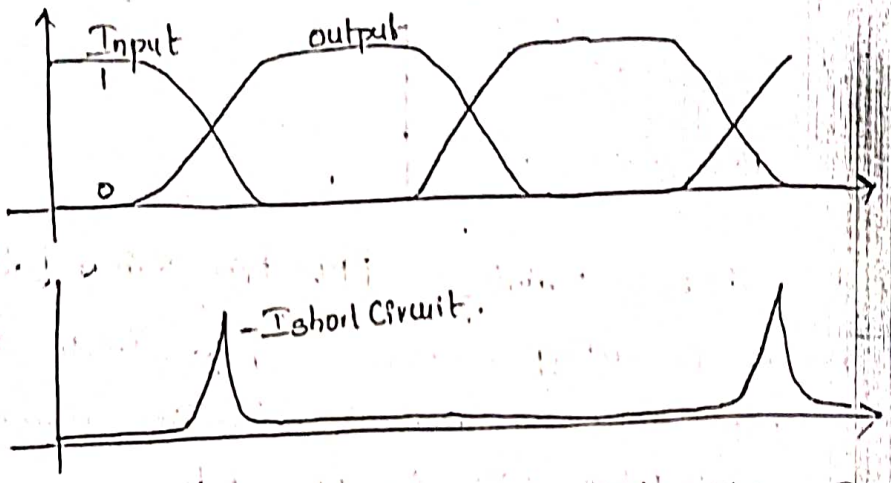
Short Circuit power dissipation :

UNIT - VI

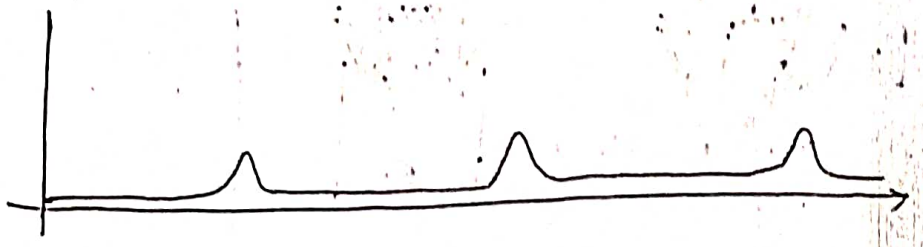


Short circuit current component flows through the both PMOS & NMOS transistors which does not contribute the charging the o/p node capacitance. Hence it is called as short circuit power dissipation.

When charging & discharging time is more then both transistor are shorted for long time.

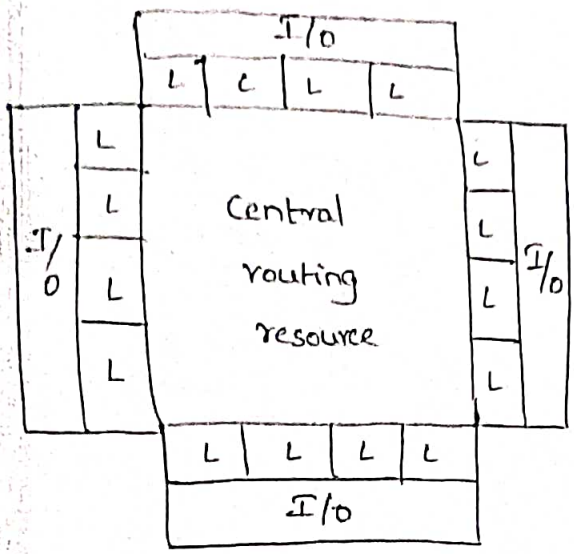


Short ckt current flows at the middle. Current compone occurs only at charging period of output but not at disch arging period. bcz. power is shown only at charging time.

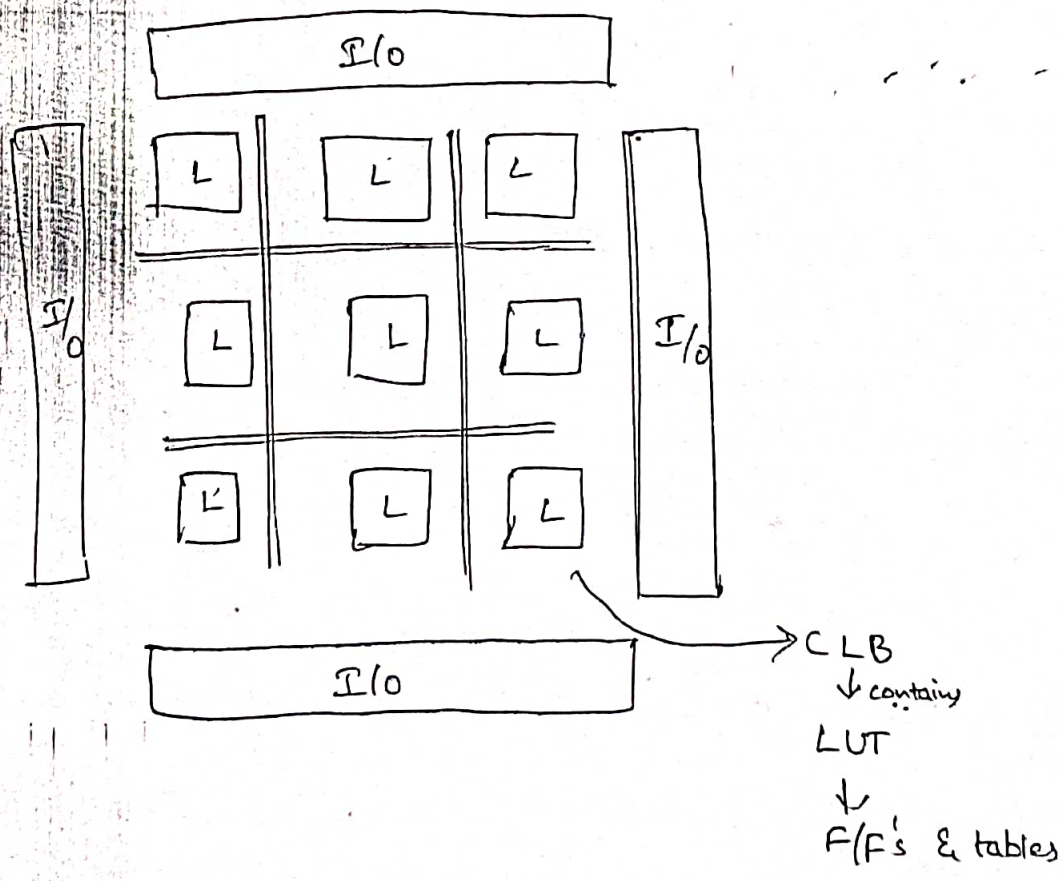


So we have reduce the spikes. So it can be reduced from first input transmission (or) increase load capacitance.

1) Increase the load capacitance.
2) Decreasing the input transition.


I/O
L
Central
routing
resource
I/O

FPGA

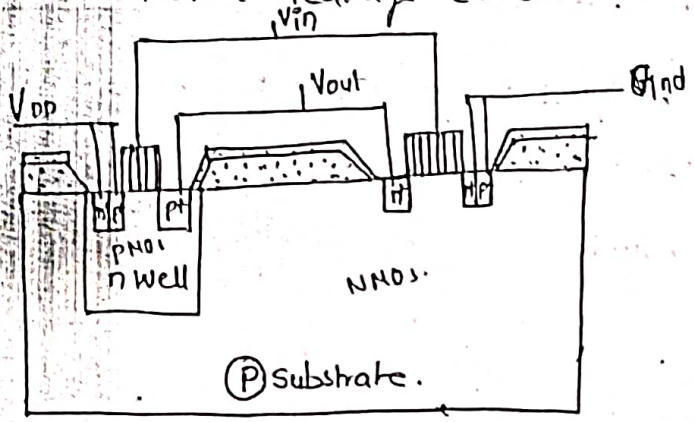

I/O
L
I/O
I/O
CLB
↓ contains
LUT
↓
F/F's & tables

Leakage power dissipation :-

When Device is in OFF (static mode) eventhough the Curren flows, then these current components are called leakage pow dissipation. Two types of Current Components, they are.

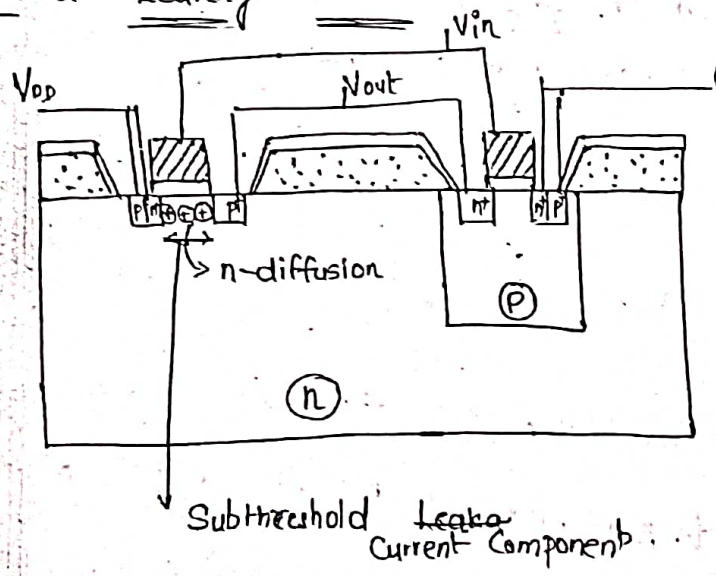
i) Diode Reverse leakage Current.

ii) Subthreshold leakage Current.



The parasitic diode is forming in PMOS b/w drain & bulk terminal and it is acting as Reverse bias diode. This Reverse bias diode draw a Reverse saturation current from the power supply when PMOS is OFF state.

Subthreshold Leakage Current :-



Subthreshold leakage Current flows when PMOS is OFF state b/w the source & Drain terminals under weak inversion layer. (Weak channel is existing b/w Drain & Source due to the diffusion).

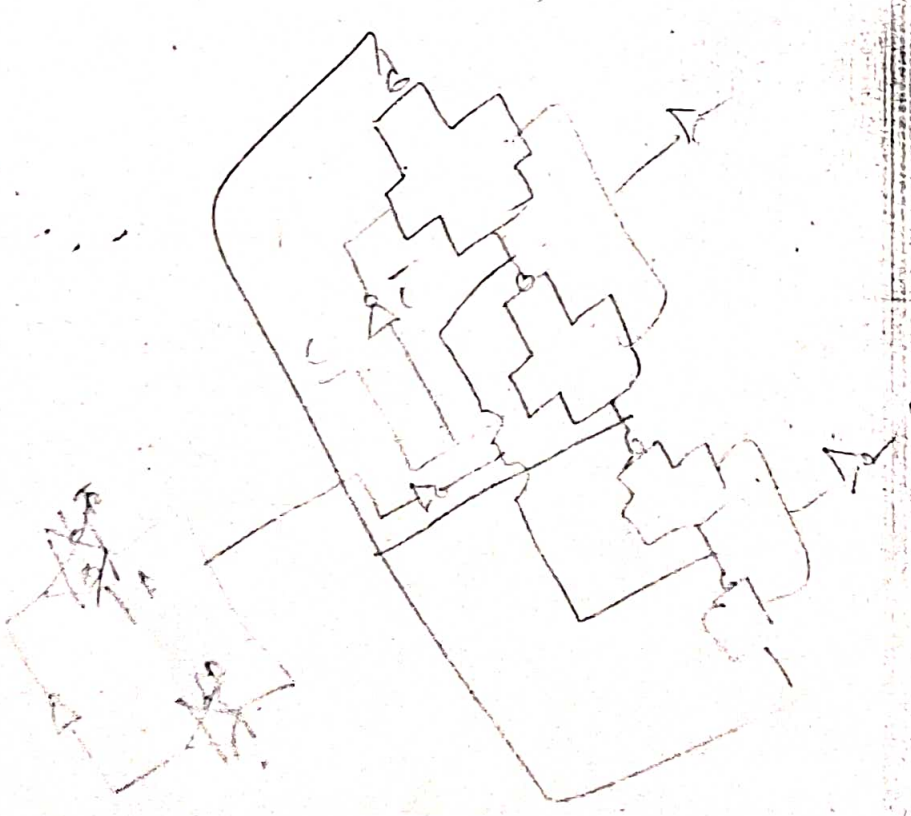
Eg:- Mobile.

Sum of

The total power dissipation is dynamic power dissipation, short circuit power dissipation, leakage power dissipation and static power dissipation.

$$P_{Total} = P_{dyn} + P_{short} + P_{leakage} + P_{static}$$

$$P_{total} = \alpha_T C_L V_{DD}^2 f + V_{DD}(I_{short} + I_{leakage} + I_{static})$$



Low power design through Voltage Scaling:

Dynamic power, $P_{dynamic} = \alpha_T C_L V_{DD}^2 f_{clk}$

C_L - Load Capacitance

V_{DD} - Supply voltage

α_T - Low Txn factor

We can achieve low power design i.e., reduced dynamic power dissipation by decreasing the supply voltage. Decreasing the supply voltage is called as Voltage Scaling or Scale down.

Influence of Voltage Scaling on Power & Delay:

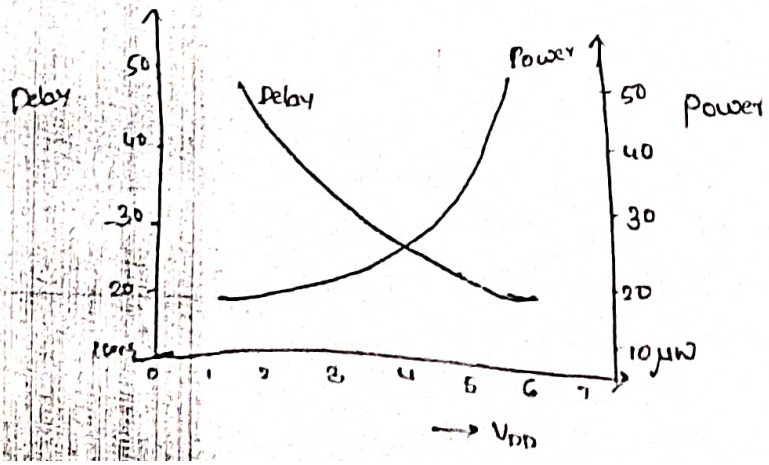
According to dynamic power expression,

$$P_{dyn} = \alpha_T C_L V_{DD}^2 f_{clk}$$

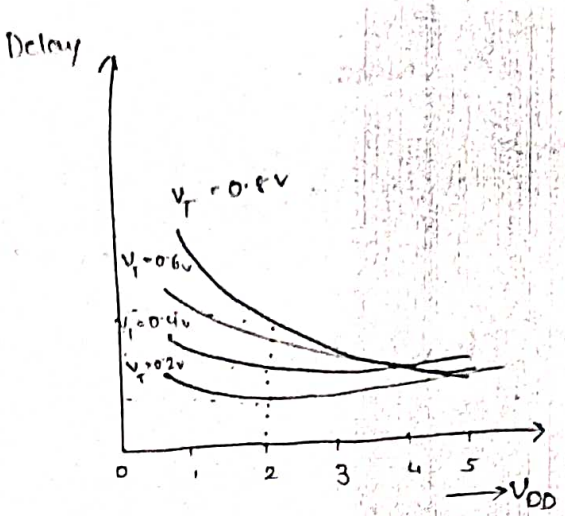
$$\Rightarrow P_{dyn} \propto V_{DD}^2$$

and also time delay (rise time) $t_r = \frac{3C_L}{\beta_p V_{DD}}$

$$\Rightarrow t \propto \frac{1}{V_{DD}}$$



Here, reduction of supply voltage decreases the dynmic power dissipation but ↑ dp time delay. So, to compensate & decrease



the time delay, decrease the threshold voltage of the device for the lower supply voltage i.e., ≃ 2V

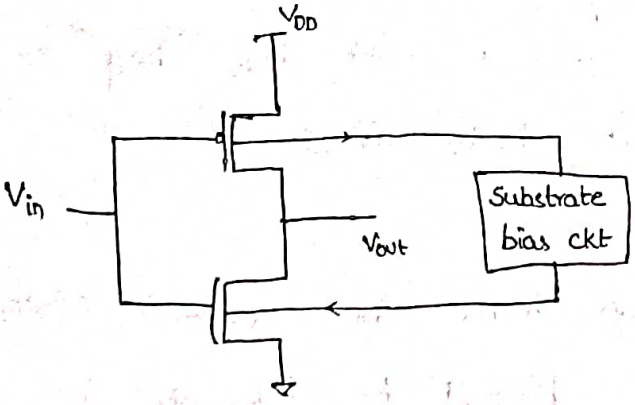
It is shown in figure ① & ②.

So, we can achieve low power design with high speed by decreasing both supply & Threshold voltage

Two techniques to avoid Sub Threshold Conduction/leakage current:

1. VTCMOS – Variable Threshold CMOS
2. MTCMOS – Multiple Threshold CMOS

VTCMOS:



Consider V_{DD} = 2V

PMOS: V_{Tp}

operating mode : −0.2V

Stand by mode : −0.6V

Bias voltage of PMOS (V_{BP})

operating mode : 2V

Stand by mode : 4V

For NMOS:

Threshold (V_{Tn}): operating mode : 0.2V

Stand by mode : 0.6V

Bias voltage of NMOS (V_{Bn}): operating mode : 0V

Stand by mode : -2V

VTCMOS means varying Threshold voltage for different modes

Advantages:

→ Operating ckt with low power / supply voltage i.e., 2V, so that it consumes less dynamic power dissipation.

→ It is operating with low Threshold voltages V_{tn}, V_{tn} i.e., 0.2 and -0.2V so that high speed can be achieved.

→ AVoid the Sub Threshold leakage current by increasing the Threshold voltages of both PMOS & NMOS Transistors. When stand by mode is OFF with the help of Substrate Bias Circuit body effect.

Disadvantages:

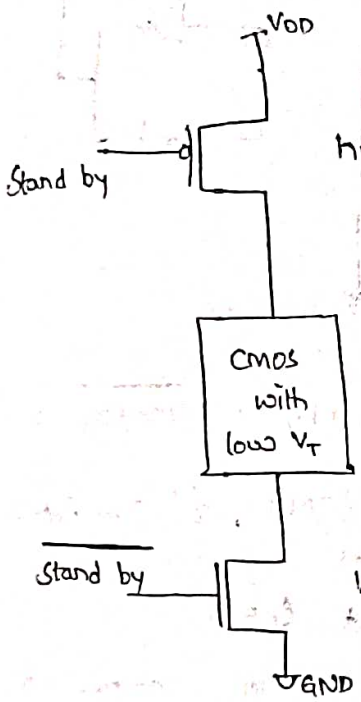
→ We need to design / form the additional substrate bias circuit. It is difficult to fabricate & control

→ It is not applicable to all Systems / designs.

→ For fabrication, we need to use high resistive wells ie; twin well / triple well process is required.

MTCMOS: Multiple Threshold CMOS

Consider a CMOS with low V_T, to achieve the low power with High Speed.



→ To avoid SubThreshold leakage

→ To achieve low power with high speed.

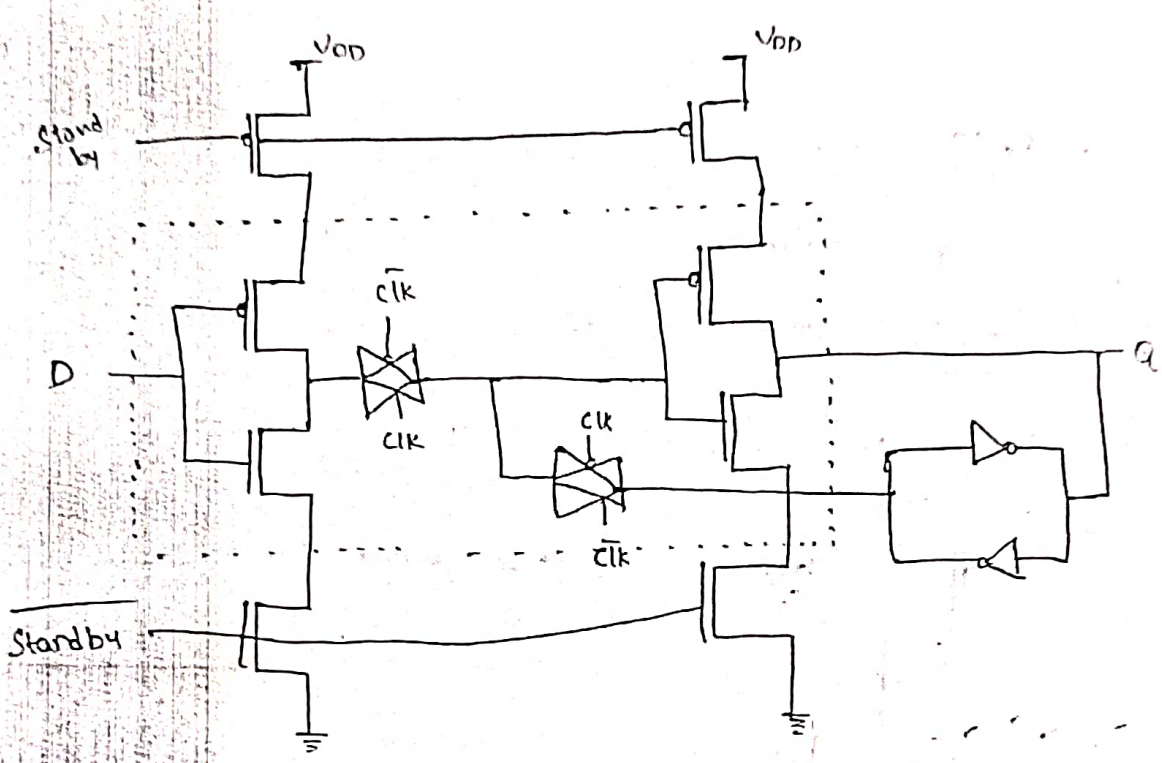
Advantages:

→ No need to use additional substrate bias ckt,

→ Disadvantages:

* No. of Transistors is more
* Two power supplies are required

Low power / Low Voltage D-latch circuit designed with MTCMOS Technique:



D	Q
0	0
1	1

When D=0, Stand by = 0, $\overline{\text{Stand by}}$ = 1,

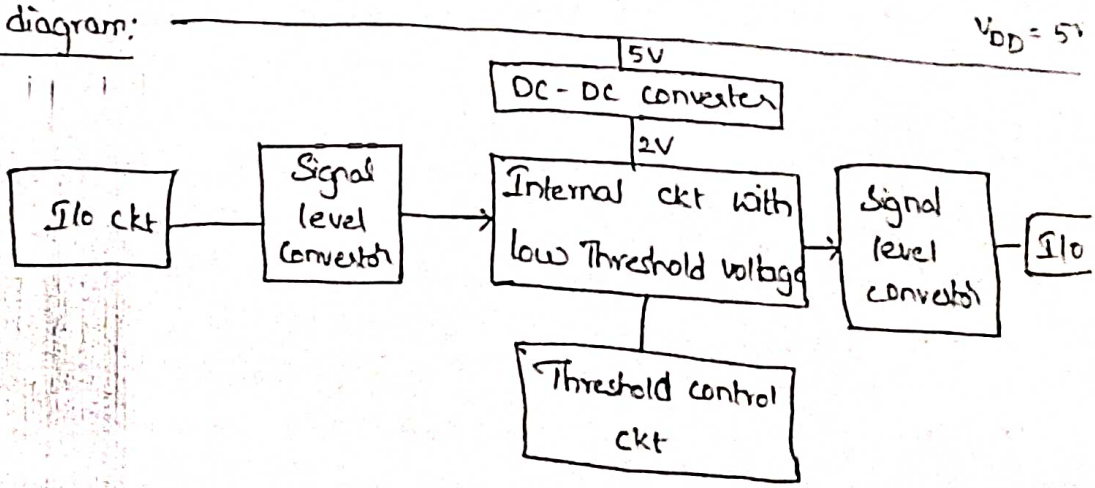
then 1st T·G (ON), 2nd Txn Gate (O
(Txn Gate)

and the output Q = 0

→ When Stand-by is 0, there is no connection with power rails

Low power chip with DC-DC convertor:

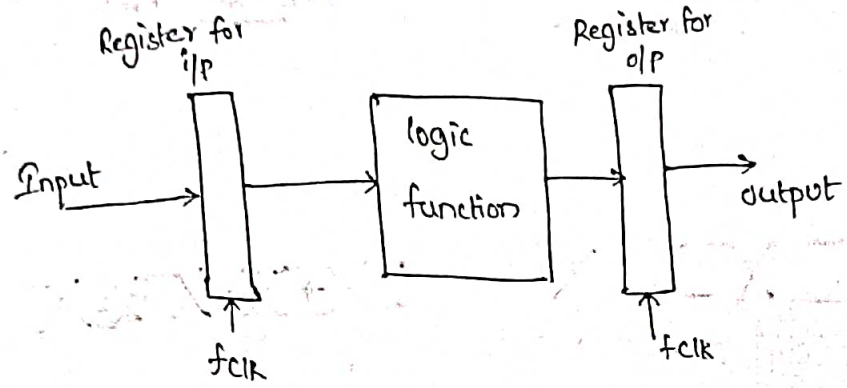
Block diagram:

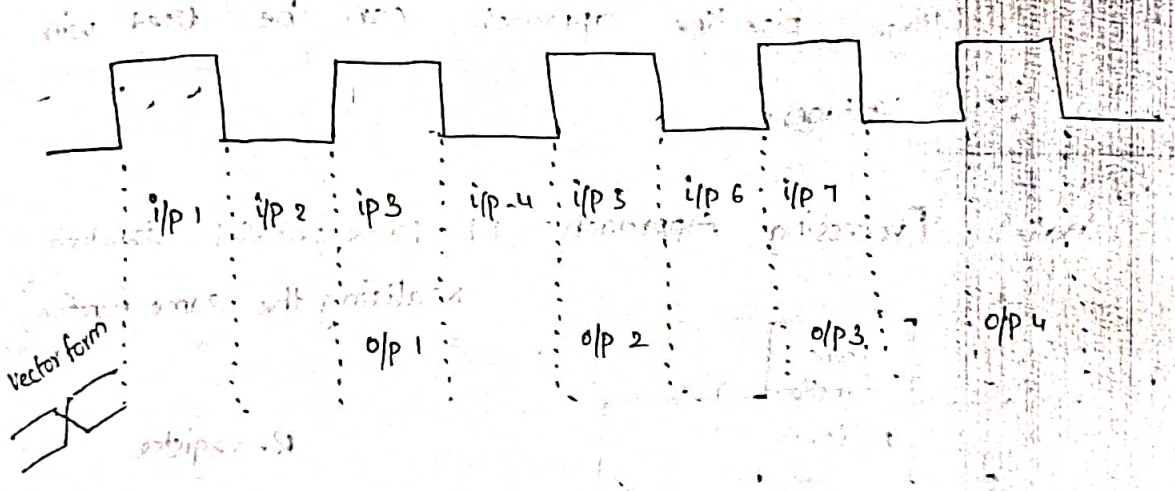


System level approaches for lowpower designs:

1. pipeline approach
2. parallel processing approach. } Generalised Techniques

1. pipeline approach:





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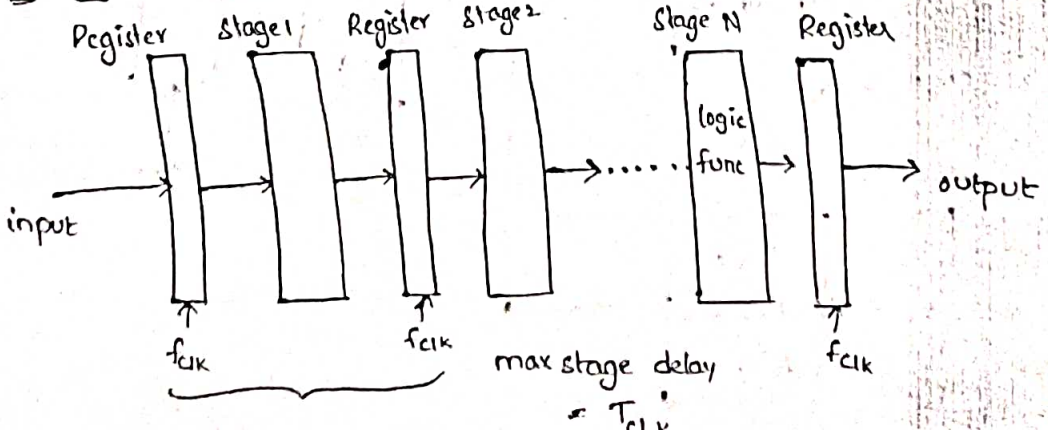
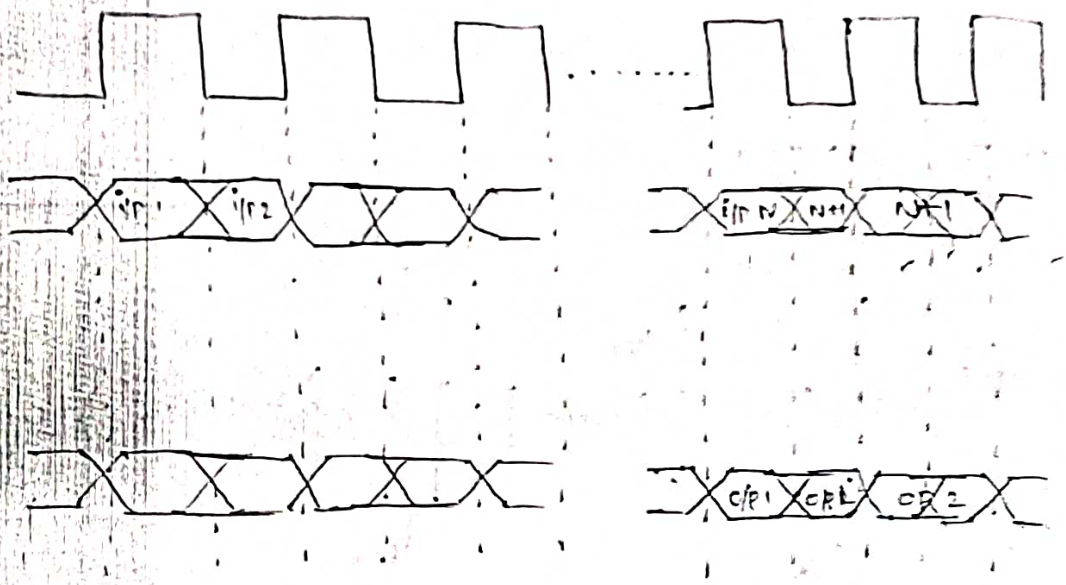
<Parallel Processing approach: Next page>,

N-Stage Pipeline Structure:

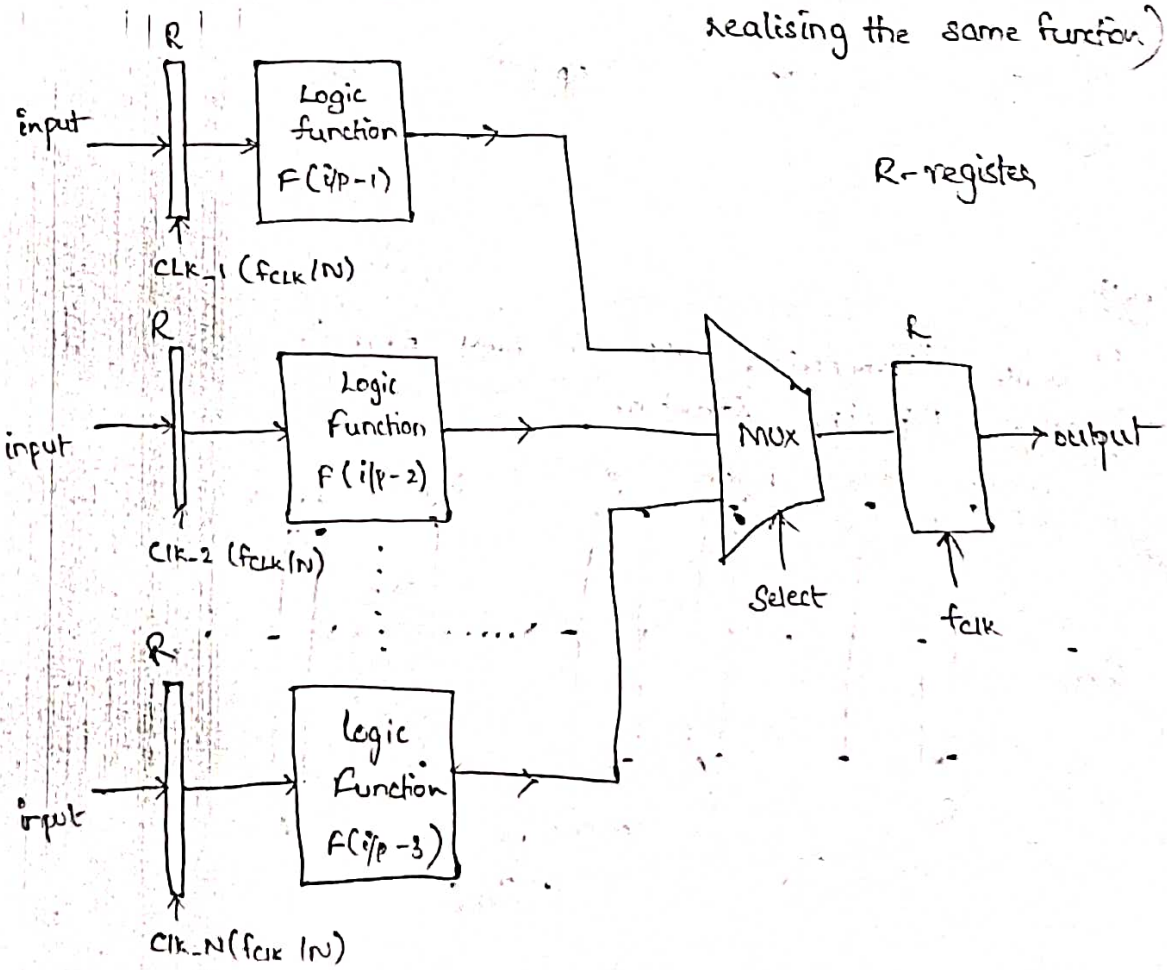


Wave forms:

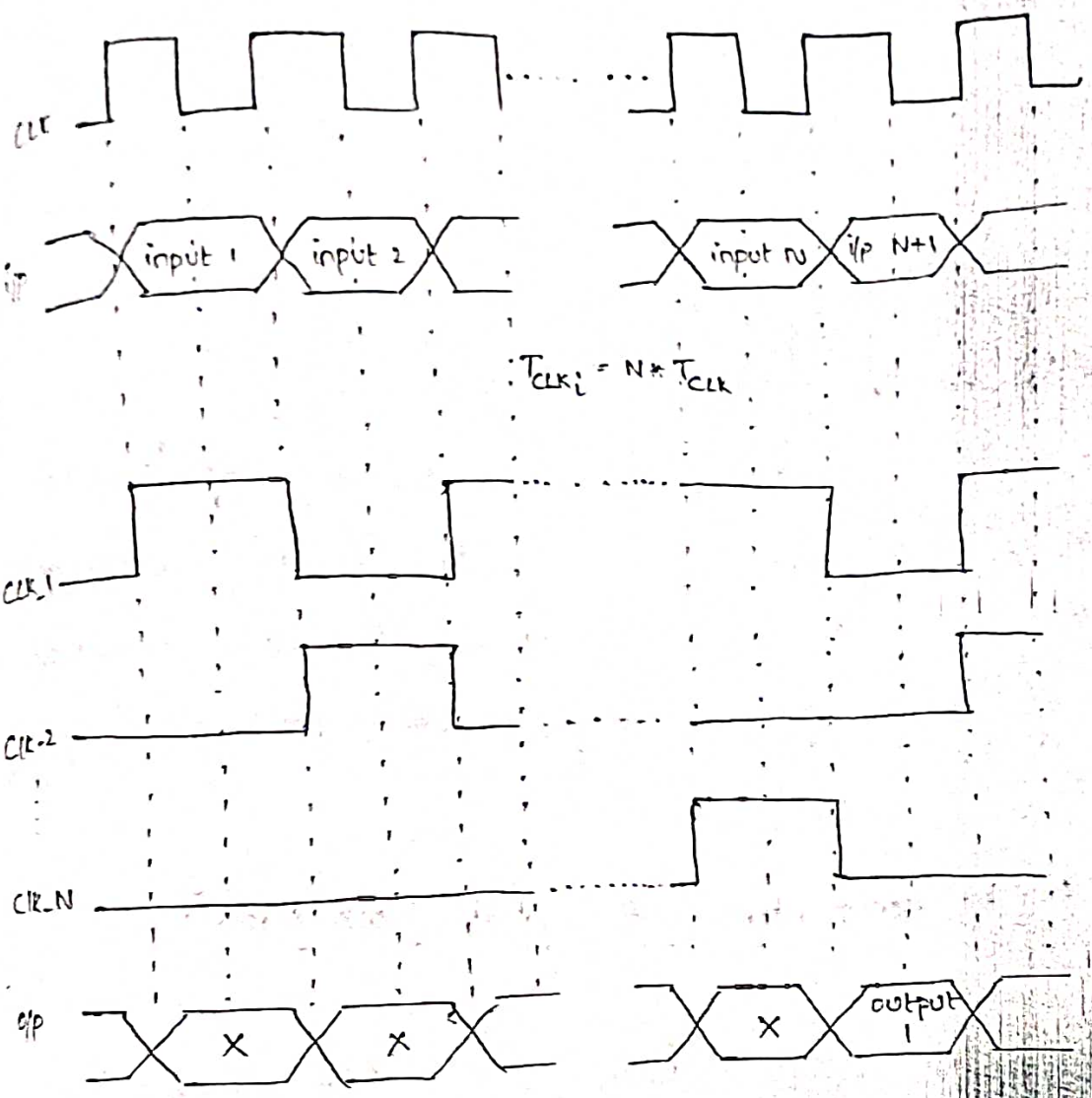


* N-stage pipeline approach can be used with low voltages.

Parallel Processing Approach: (N- block parallel structure realising the same function)



Timing diagram of N- block parallel Structure:



* pipeline approach are not low power techniques

* Estimation of Switching activity & reduction of Switching activity:

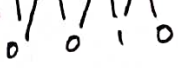
Binary to gray: 0 0 1 0 → 0 0 1 1

On Node Transition:

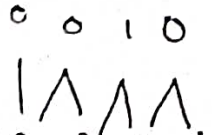
Gray Code : 1: 0 0 0 1

To Binary

3: 0 0 1 1



2: 0 0 1 0



(one bit change code)

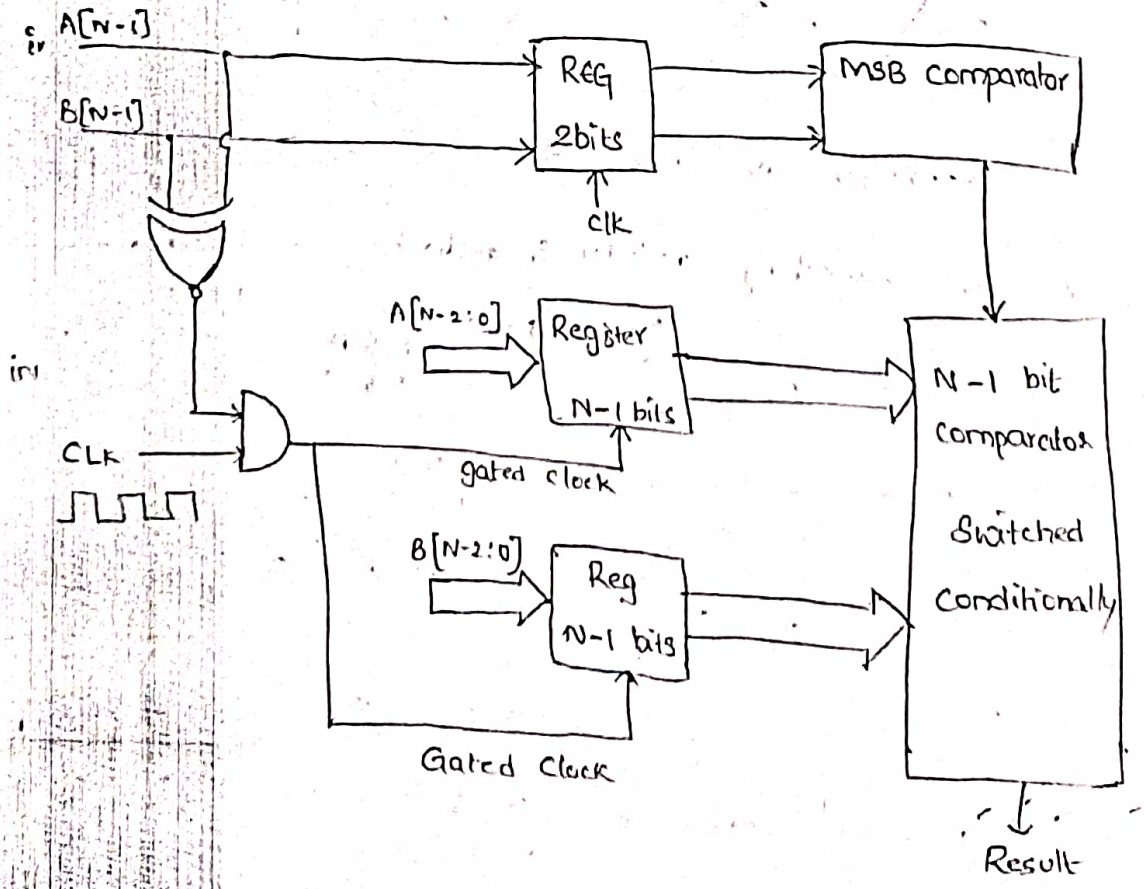
To reduce No. of Switching activities

1. Algorithm level - 2's comp, Gray code
2. Architectural level
3. proper selection of logic topologies
4. Circuit level optimisations.

-Algorithm level

For representing -'ve nos, we use signed magnitude representation instead of 1's complement & 2's complement. Use Gray code for representing i/p & o/p patterns. Use diff. optimising techniques like FFT, DFT we use the

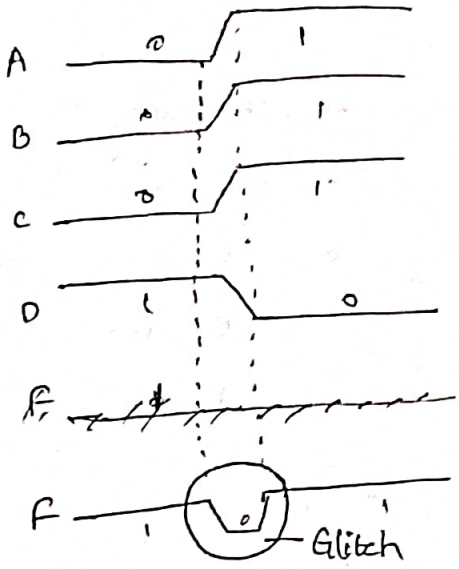
N-bit comparator with gated clock signal:

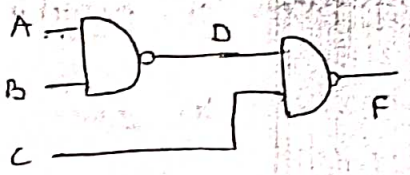


A - 1010

B - 0111

If the MSB bits are different, o/p of XNOR is '0' & hence the gate o/p is '0' resulting in disabling the 2 digit registers. Only MSB bits are compared. in MSB comparator & result is obtained directly





Glitch is a noise peak. It is occured due to the imbalance of impedance & Gate delays.

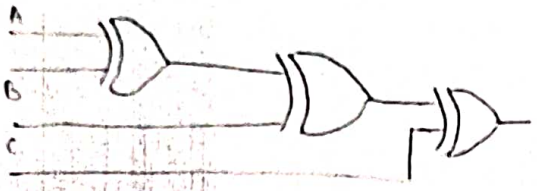
By reducing these glitches, we can save power.

(Glitches cane be reduced using parity ckts)

Glitches can be avoided by changing structure of the ckt.

Ex: Consider parity ckt.

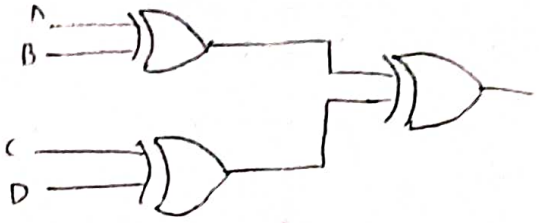
Chain Structure



more delay

→ Glitches are more

Tree Structure

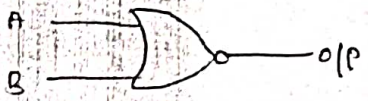


less delay

→ Glitches can be reduced.

Estimation of Switching activity:

Consider Nor Gate



A	B	o/p
0	0	1
0	1	0
1	0	0
1	1	0

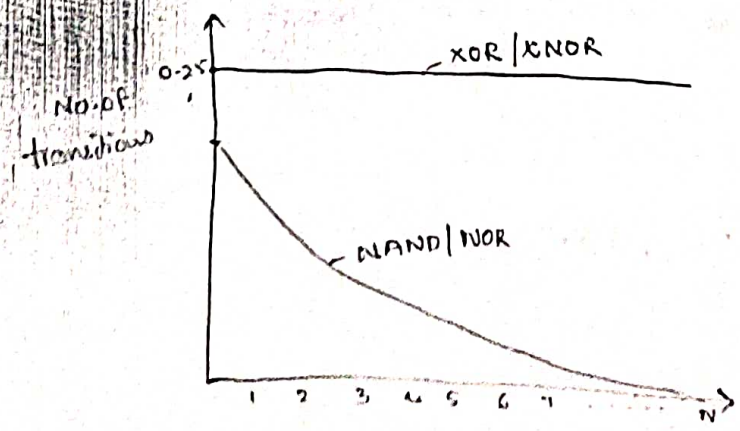
probability of getting logic '1' – $\frac{1}{4}$

logic '0' – 3/4

→ Probability of Total No. of transitions at o/p is Product of probability of logic '1' & logic '0'

→ Here probability of transitions = $\frac{1}{4} \times \frac{3}{4}$ (or) $\frac{3}{16}$ //

If No. of i/ps ↑, No. of transitions probability ↓.



XOR $\frac{2}{4} \times \frac{2}{4} = \frac{1}{4}$

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Manchester Carry Chain Adder:

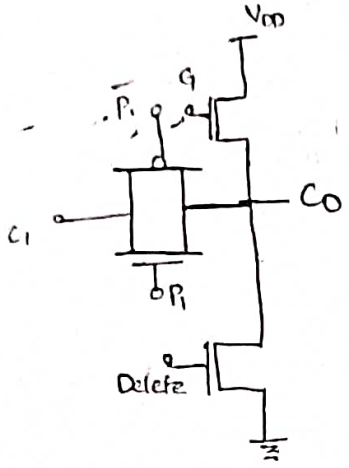


fig (a)

static, using propagate, generate & kill

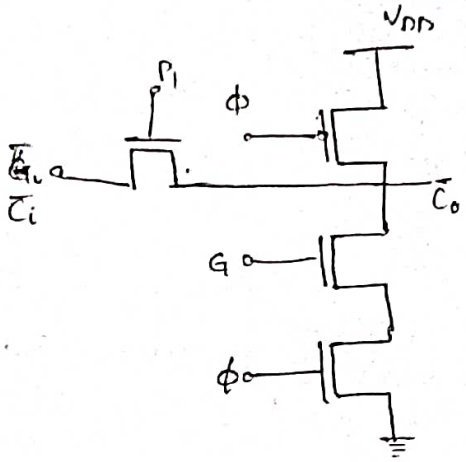


fig (b)

Dynamic implementation using only propagate & Generate signals.

ϕ – clock

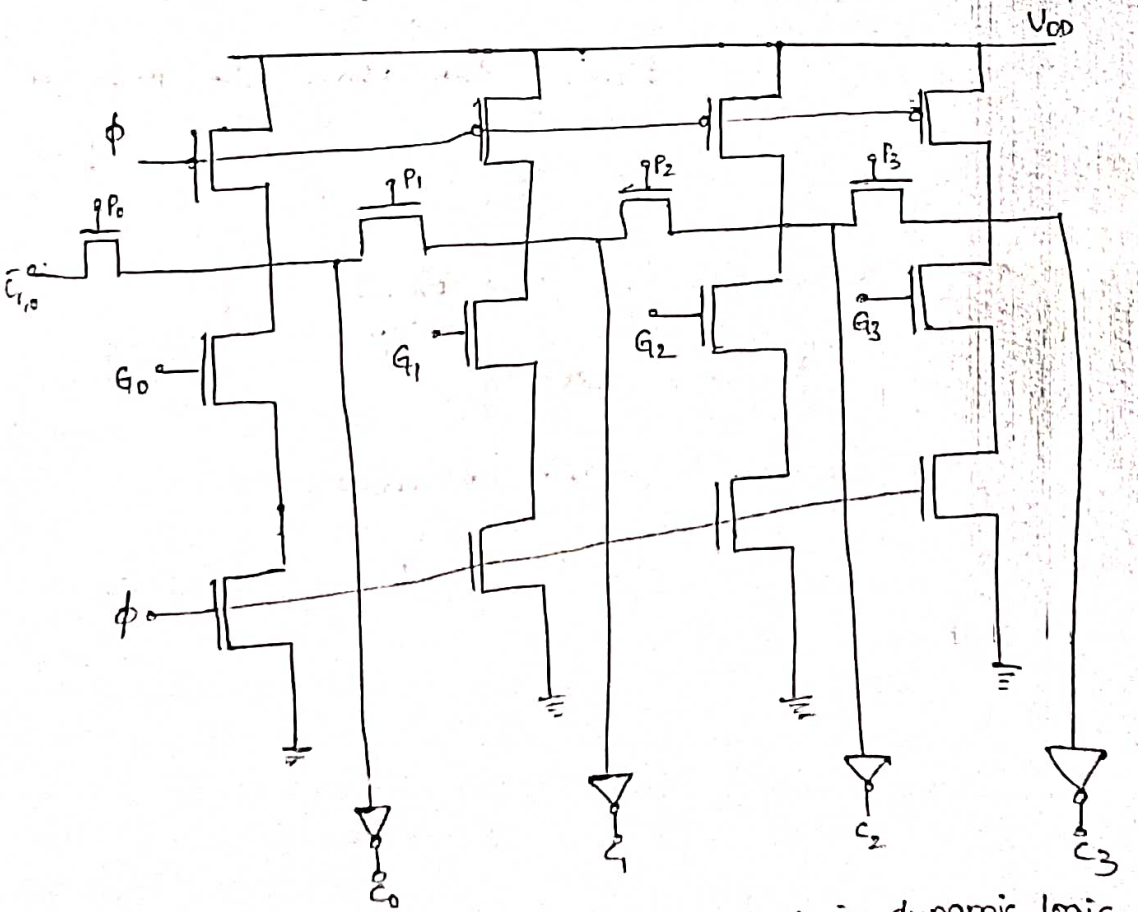


figure: Manchester carry-chain adder in dynamic logic (4 bit section)

Propagate signal, $P = A \oplus B$

Generate signal, $G = A \cdot B$

If Generate signal G is '1', o/p carry is 1

If P is '1', i/p carry is propagated to o/p.

→ fig (a):

When $P_i = 1$, the Transmission Gate is ON & the c_i is propagated to C_o.

When $G = 1$, the NMOS is ON & o/p $C_o = V_{DD}$ = logic '1'.

Where we want to delete, delete signal is given at the NMOS (bottom).

→ fig(b): Two phases in dynamic logic

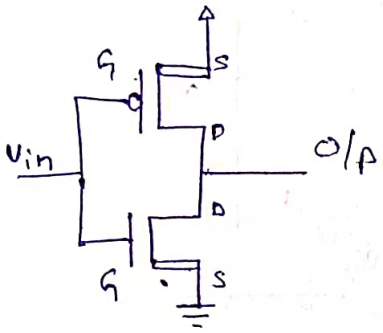
1. precharge phase: During this phase, o/p node gets charged. (when $\phi = 0$)
   → It doesn't decide the o/p.
2. Evolution phase: decides the phase (like drivers) o/p ckt
   → towards discharge path.

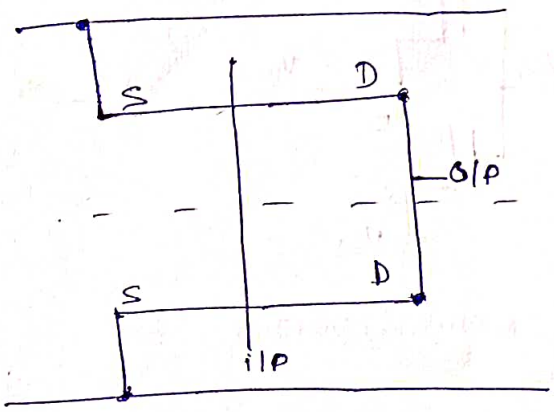
* If P_i is '1', o/p carry = i/p carry.
* If G is '1' & ϕ is 1, o/p $\overline{C_o} = 0 \Rightarrow C_o = 1$ (satisfied)

VLSI Assignment-I

D. Saivenkat
19091A04H4
ECE, B/s

1. Draw the stick diagram of P-well cmos inverter





2. write the comparative aspects of key parameters of cmoss and bipolar transistor.

ans Following are the characteristics of bipolar technology.

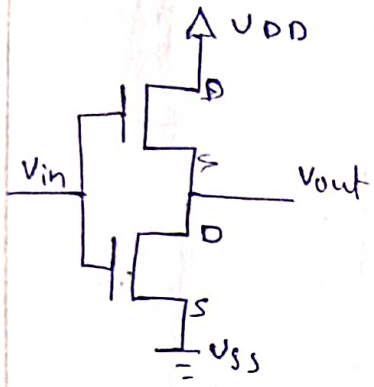
i) Higher switching speed.
ii) it offers high current drive per unit area and high gain
iii) Generally better noise performance and better frequency characteristics
iv) Low packing density.
v) Low voltage swing logic.

CMOS :-

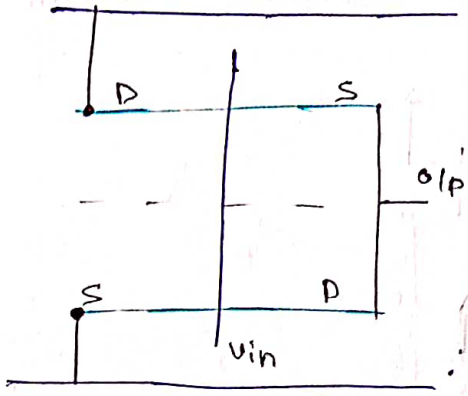
Benefits of cmos Technology.

i) It offers noise margins
ii) offers high packing density
iii) It has low manufacturing cost per device
v) scalable threshold voltage
vi) It has high i/p impedance.

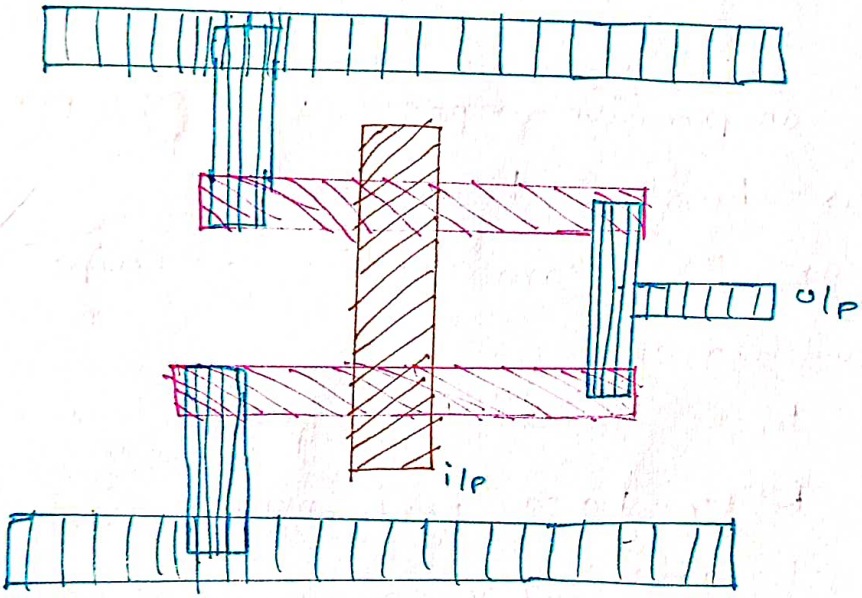
3 Draw the stick diagram and layout for dep & mode nmos transistor.



NMOS invertor



stick diagram



layout:-

4 Define Integrated resistance and capacitance.

Integrated resistance

In general, a resistor is used to control the current flow of other electron components in a IC device

Integrated capacitance :-

The Base collector diviction of a transistor without emitter diffusion can be used as a capacitor. the emitter Base junction can b

as an N region can be diffused into one of the p isolation region during an emitter diffusion.

5 Give advantages of Bicmos over cmos

i) improvd Speed over cmos
ii) Flexible inputs and outputs.
iii) High performance analogs
iv) Latchup immunity [1:2]
v) Lower power dissipation than Bipolar.

6. what is transistor sizing?

A. The sizing of the transistor can be done using Rc delay approximation. The Rc delay model approximates a transistor as a switch with a series of resistances as effective resistance R The size of a unit transistor is approximated as 4/2d

7 Derive the expression for I_{ds} for N-channel mosfet in linear region.

A:- The expression for I_{ds} for N-channel MOSFET in linear region is

charge $Q = CV$; $C = \frac{\varepsilon A}{d}$

and $Q = It$

$I = Q/t$

$$T = \frac{L}{v} \qquad v = \mu E = \mu \frac{V_{ds}}{L}$$

$$= \frac{L}{\mu \frac{V_{ds}}{L}}$$

$$T = \frac{L^2}{\mu V_{ds}} \longrightarrow (1)$$

Charg induced in the channel

$$C = \frac{\epsilon A}{d}$$

$$Q = CV$$

$$= \frac{\epsilon_0}{t_{ox}} \left\{ (V_{gs} - V_t) - \frac{V_{ds}}{2} \right\}$$

$$Q = \frac{\epsilon (w.L)}{t_{ox}} \left\{ (V_{gs} - V_t) - \frac{V_{ds}}{2} \right\} V_{ds}$$

$$\frac{(2)}{(1)} \Rightarrow I = \mu \left(\frac{\epsilon}{t_{ox}}\right) \frac{W}{L^2} \left\{ (V_{gs} - V_t) - \frac{V_{ds}}{2} \right\} V_{ds}$$

$$\boxed{I_{lin} = \mu C_{ox} \left(\frac{W}{L}\right) \left\{ (V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right\}} \longrightarrow (3)$$

8 Derive the expression I_{ds} for N-channel mosFET in the saturation region.

Ans: In saturation region :-

$$T = \frac{L^2}{\mu V_{ds}} \longrightarrow (1)$$

$$Q = \frac{\epsilon (WL)}{t_o} \left\{ (V_{gs} - V_t) - \frac{V_{ds}}{2} \right\} \longrightarrow (2)$$

(1) & (2) equations

$$V_{ds} = V_{gs} - V_t$$

from equation (3) the linear saturation region.

is

$$I_{sat} = \mu C_{ox} \left(\frac{W}{L} \left\{ (V_{gs} - V_t)(V_{gs} - V_t) - \frac{(V_{gs} - V_t)^2}{2} \right\} \right.$$

$$= \mu C_{ox}\left(\frac{w}{L}\right)\left\{(V_{GS}-V_t)^2 - \frac{(V_{GS}-V)^2}{2}\right\} \quad \ldots\rightarrow (3)$$

Assume $\mu C_{ox}\left(\frac{w}{L}\right) = k$

$$I_{sat} = k\left\{\frac{(V_{GS}-V_t)^2}{2}\right\}$$

The gate effective capacitance $C_g = C_{ox}(W \times L)$ substitute in this eq (3) $I = \frac{\mu C_g}{L^2}\left\{\frac{(V_{GS}-V_t)^2}{2}\right\}$

9 Explain the term Lithography

Lithography is the heart of the semiconductor production process. It is used to fabricate electrical devices by the patterning specific forms of a thin layer on a hard substrate. The direct and monolithic integration of numerous layer on a water producer the devices.

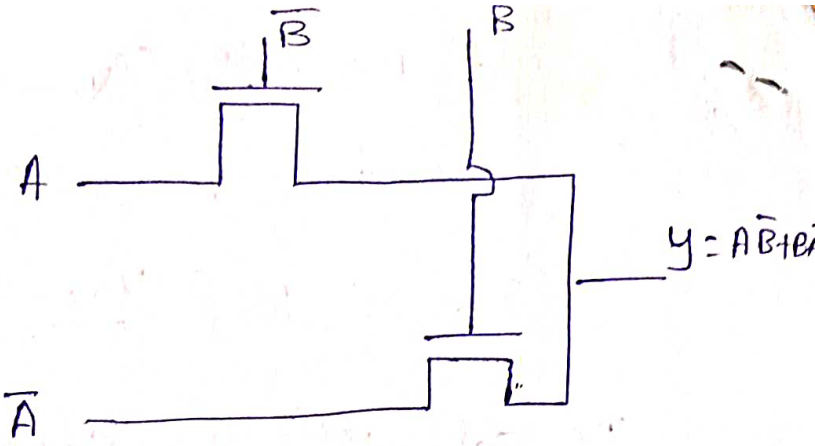
10 Explain the term Ion Implantation?

Ion Implantation is a low-temperature technique for the introduction of impurities into semiconductors and offers more than flexibility than diffusion for instance in mos transistors, Ion implantation can be used to accurately adjust the threshold voltage.

11 Draw the pass transistor logic for EX-OR and NAND?

Truth table Ex OR

A	B	y
0	0	0
0	1	1
1	0	1
1	1	0

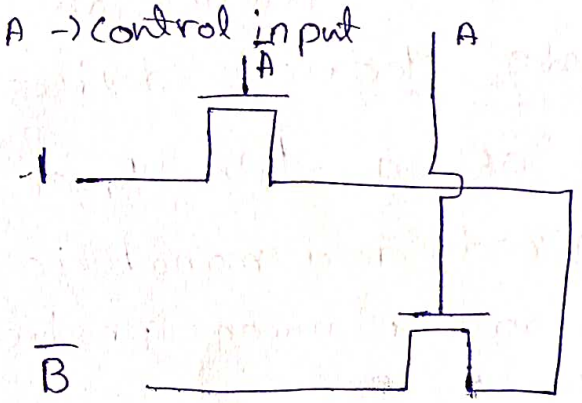


0 = B

1 = B

for NAND gate

A	B	y
0	0	1
0	1	1
1	0	1
1	1	0



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ECE - D/S.

VLSI.

Assignment - 2

(1) Explain pipelining and parallel processing approach in detail?

In certain types of applications variable threshold voltage & multiple threshold are infeasible due to technological limitations.

The above problem can be rectified by using system level architecture measures such as:

i) pipelining approach
ii) parallel - process approach

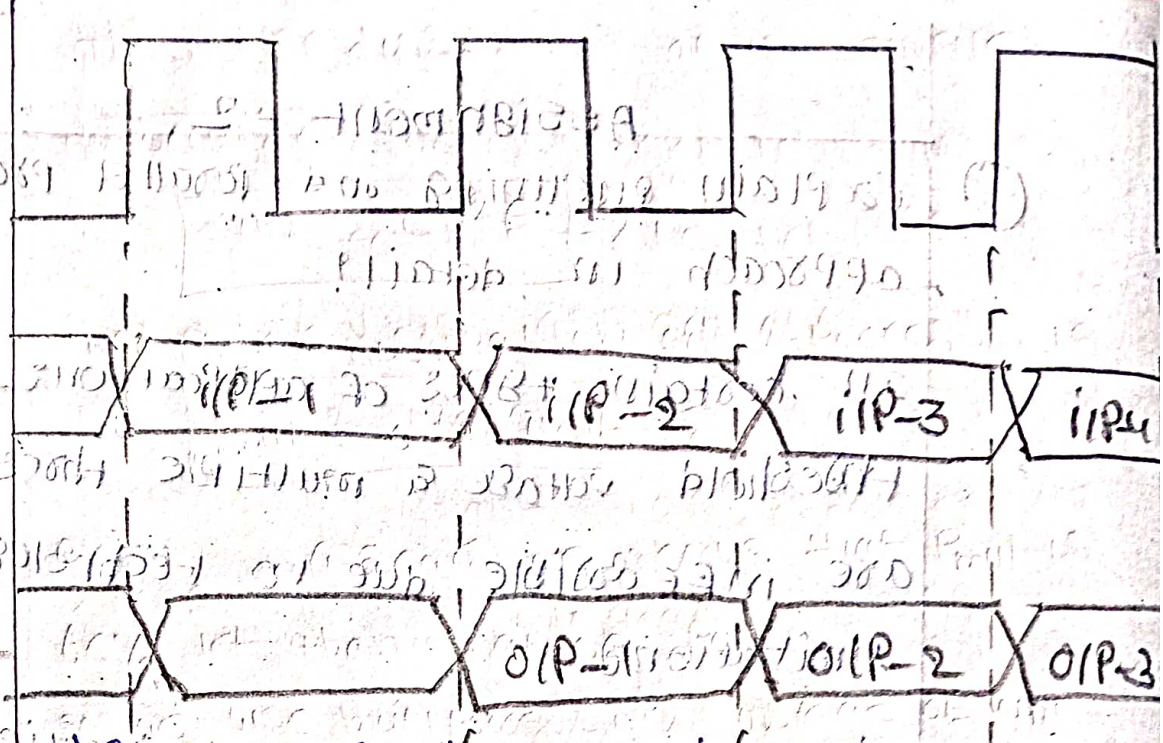
(i) Pipelining approach:-

In this approach both I/P & O/P vectors are sampled through input register driven by a clk signal.

The maximum I/P to O/P propagation delay of the logic block is equal to less than

$$T_{CLK} \geq \frac{1}{f_{CLK}}$$

→ The I/P vector is latched into the I/P register array to each clock cycle and O/P data becomes valid with a latency of one cycle.



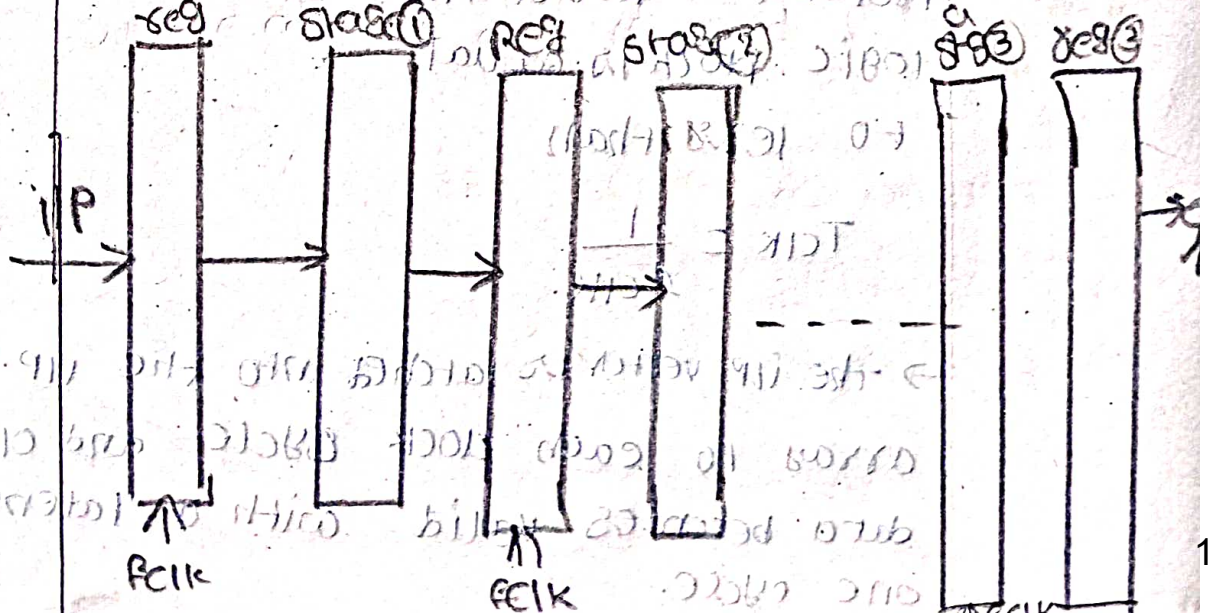
the above fig shows the single-stage implementation of a logic function and its simplified timing diagram

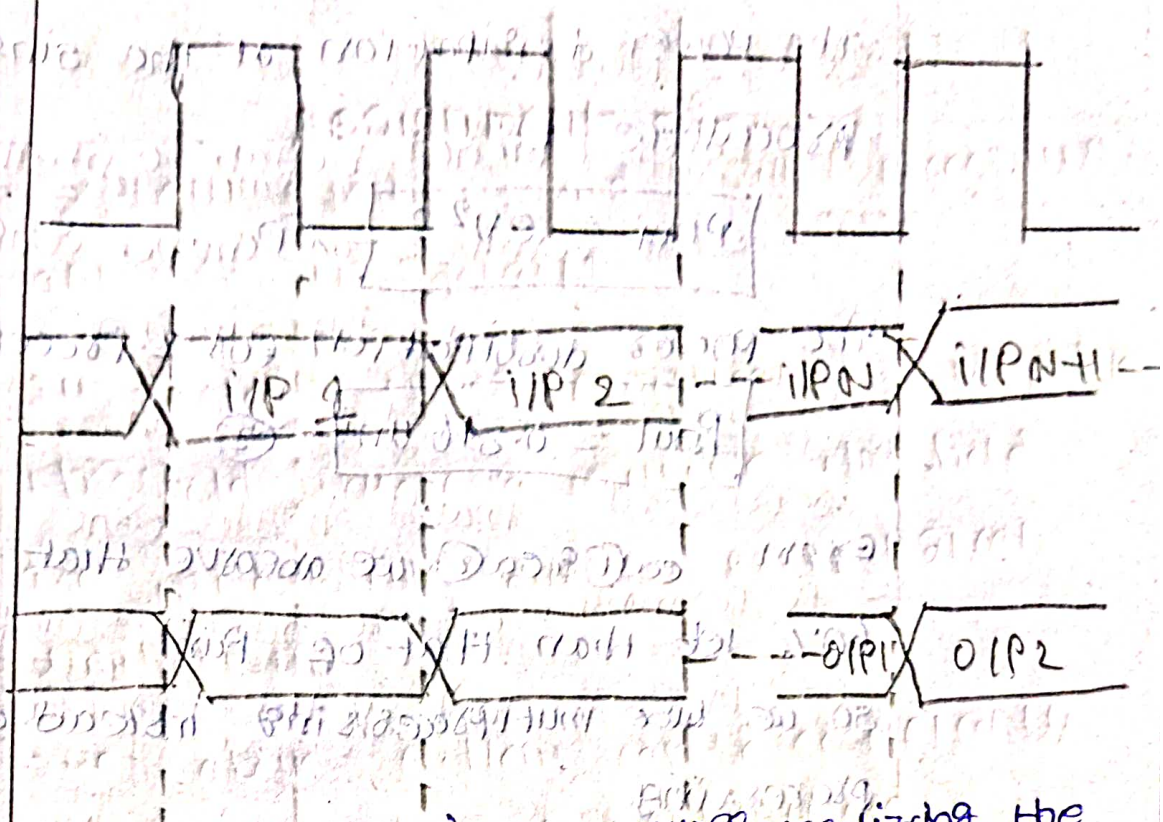
$\therefore C_{Total} = C_{registers(i/p)} + C_{logic\,fun} + C_{o/p\,regist}$

$P_{ref} = C_{Total} \cdot V_{DD}^2 f_{clk}$.

N-stage pipeline structure:

there (N+1) registers are increased, therefore (N-1) capacitance are increased in order to reduce the power.





→ N-stage pipeline structure realizing the logic function

→ the maximum pipeline stage delay is equal to clock period & the latency is 'N' clock cycles.

→ the dynamic power consumption of N-stage pipeline.

$$P_{pipeline} = [C_{Total} + (N-1)C_{reg}] V_{DD}.new^2 f_{CLK}.$$

parallel processing approach:

consider 'N' identical processing elements each implementing the logic function F in parallel.

Assume that the consecutive input vectors arrive at the same rate as in the single stage case = The input vectors are routed to all the registers of the N-processing block.

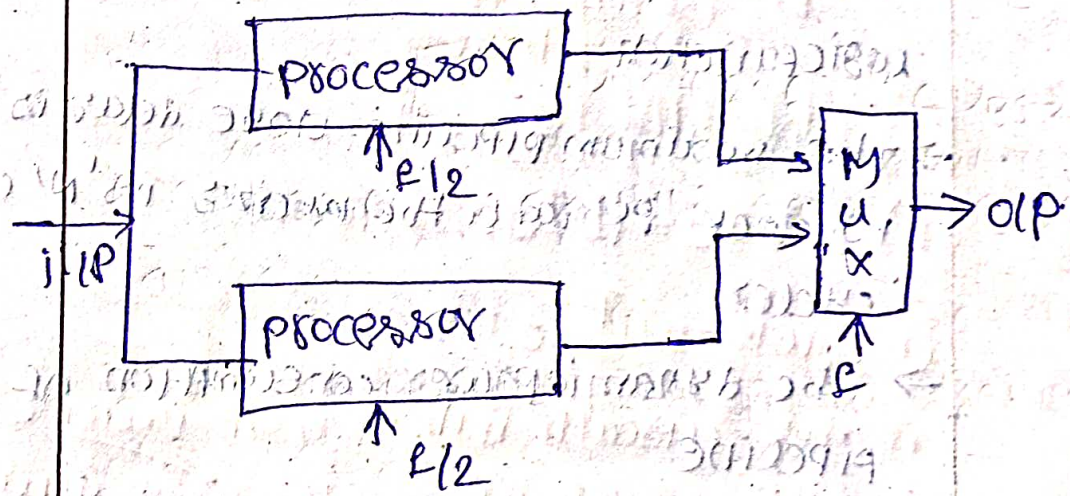
The power dissipation at the single processor is

$$P_{uni} = CV^2f \rightarrow (1)$$

The power dissipation for 2-processor is

$$P_{mul} = 0.396\, P_{uni} \rightarrow (2)$$

From eqn (1) & eqn (2) we observe that P_{mul} is 60% lot than that of P_{uni} so we use multiprocessing instead of uni processing.



Draw backs.

⇒ Requires more space

⇒ more cost is also required

(2) Explain different MOS device models (L1, L2, L3, BSIM3).

MOS device modeling continue to pose a challange especially for high frequency operation.

The main objective of MOS device model is develop its base understanding of some of models to the extent necessary for simulations.

Level 1 Model :-

Level 1 model is also known as the Shichman and (Hodges model.)

$$\omega KT, I_D = \frac{1}{2} KP \frac{W}{L-2L_D} (V_{GS}-V_{th})^2 (1+\lambda V_{DS})$$

the model does not include subthreshold conduction or any short channel effects.

C_{MS} abruptly changes from $(2/3)WLC_{OX}$ - WC_{OX} in saturation to $(\frac{1}{2})WLC_{OX}$ + WC_{OX} in the bride region.

If the device operates at the edge of saturation then

$V_{GS} - V_{DS} = V_{TH}$

$C_{MS} = (2/3)WLC_{OX} - WC_{OX}$ and } triode region

$C_{MD} = WC_{OX}$

Level 2 Model :-

The Level 1 model began to manifest its short comings as channel length fell down below approximately 4um. The level 2 model was developed represent many high-order effects

→ Performing the integration with a varying threshold voltage yields

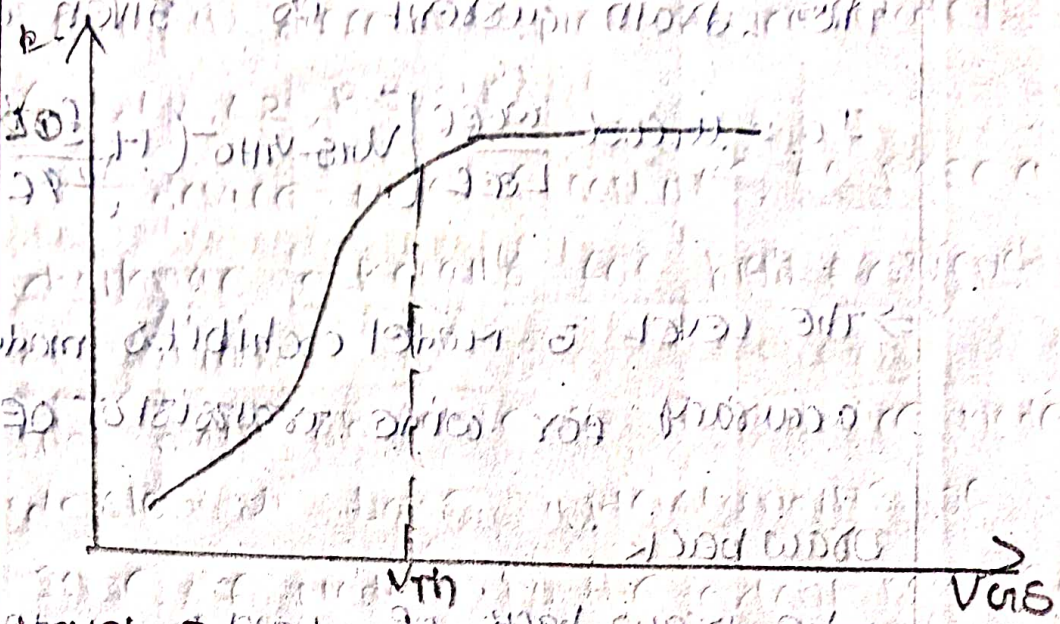
$$I_{D2} = \mu C_{ox} \frac{W}{L} \left\{ (V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} - \frac{2}{3}\gamma \left[(V_{DS} - V_{BS} + 2\phi_F)^{3/2} - (-V_{BS} + 2\phi_F)^{3/2} \right] \right\}$$

for $V_{BS} \geq 0$ I_D exhibits same dependence on 'r'

In the saturation region the drain current I_{DS}

$$I_{DS} = I_{DSat} \frac{1}{1 - \lambda V_{DS}}$$

⇒ The principal difficulty in above approach is that both the drain current and its derivative are discontinuous at the edge of triode region.



Level 3 Model :-

In Level 3 Model many empirical constants are introduced to improve the accuracies for channel lengths as small as 1 μm.

⇒ This Model expresses the threshold voltage as

$$V_{TH} = V_{THO} + F_S F_{GT}\sqrt{2\phi_F - V_{BS}} + F_n(2\phi_F - V_{BS}) + \frac{8.15\times10^{-22}}{C_{ox}L_{eff}}$$

F_S = Short channel effects

F_n = narrow channel effects

The mobility equation is involve with the vertical & lateral field effects and is represented as.

$$\mu_{eff} = \frac{\mu_{eff}}{1 + \frac{\mu_{eff} V_{DS}}{V_{max} L}}$$

$$\mu_{eff} = \frac{\mu_n}{1 + \theta(V_{GS} - V_{TH})}$$

The drain current is given as

$$I_D = \mu_i C_{OX} \frac{W_{eff}}{L_{eff}} \left[V_{GS} - V_{TH0} - \left(1 + \frac{F_{SV} + F_0}{2\phi_F - V_{BS}}\right) \frac{V_{DS}}{2} \right] V_{DS}$$

⇒ The level 3 model exhibits moderate accuracy for wide transistor of I_D.

Draw back:

The draw back of Level 3 model it is discontinuity of derivative of I_D w.r.t V_{DS} at the edge of the triode region.

BSIM series:

The feature of BSIM is the addition of a simple equation to represent the geometry dependence of many of the device parameters. The general expression from the

$$P_0 = P_{0-Ap} \cdot \frac{B_p}{L_{eff}} \cdot \frac{}{W_{eff}}$$

Improvements over Level 3 vision:

① Dependence of mobility upon the vertical field includes the substrate voltage

② The threshold voltage is modified for substrate with non-uniform doping

③ The next model IN BSIM series is BSIM2. For short narrow transistors

4. The next generation BSIM3 requires 180 parameters for channel length as low as 0.25 μm

5. BSIM3 provides resonable accuracy but still suffers from large errors in predicting the O/P impedence

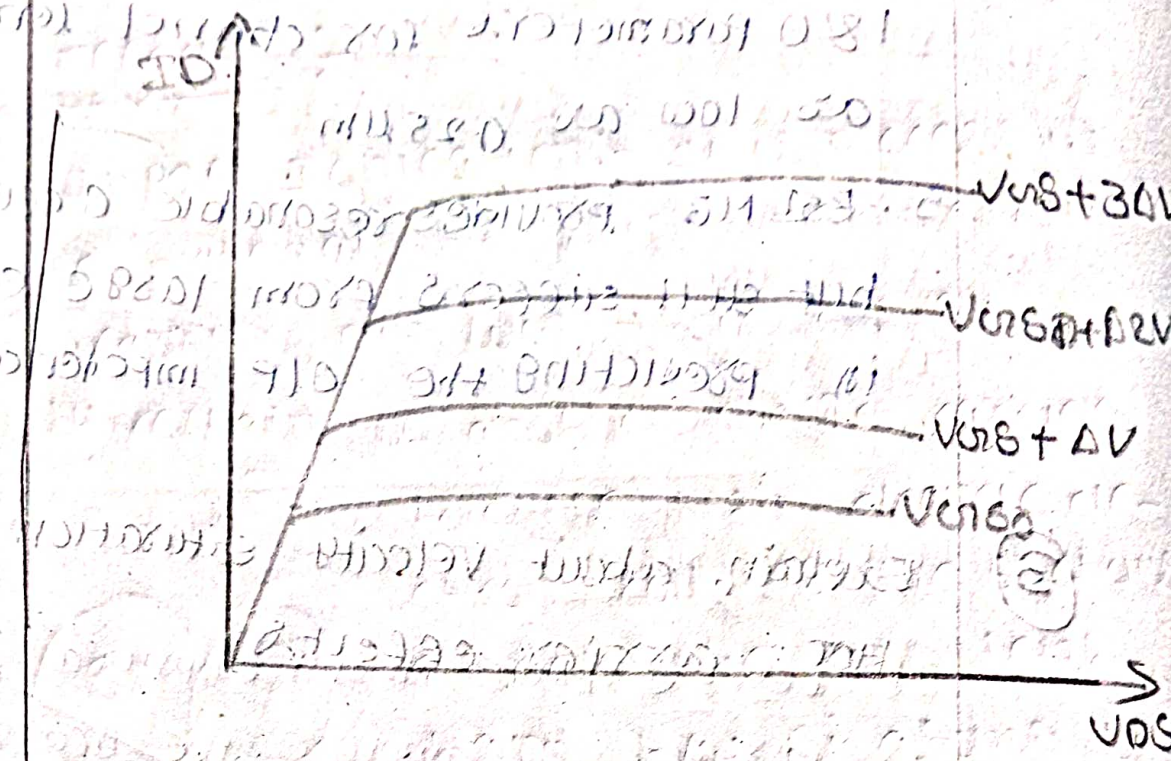
(3) Explain about velocity saturation and hot carrier effects.

Velocity saturation:

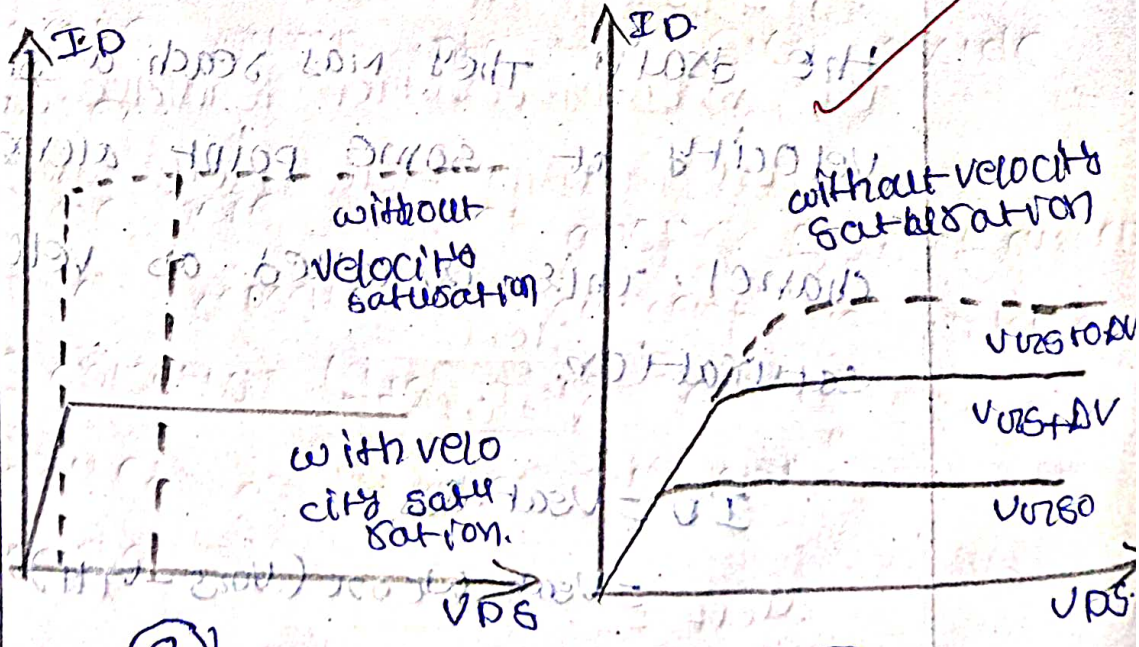
The mobility of carriers also depends on the lateral electricfield in the channel begining to drop as the field reach levels of 1V/μm. ω·KT v = με

Thus as carriers enter the channel from the source and accelerate towards the drain. They may reach a saturation velocity at some point along the channel. This is called as velocity saturation.

$$I_D = v_{sat} \cdot Q_d$$
$$= v_{sat} W C_{ox} (V_{GS} - V_{TH})$$



under typical bias conditions MOSFET's experience same velocity saturation, displaying a characteristics b/w linear and square law behaviour. VDS increases the drain current saturates well before pinch-off occurs.



(a) Premature drain current

(b) Reduction of transconductance

HOT carrier effect:

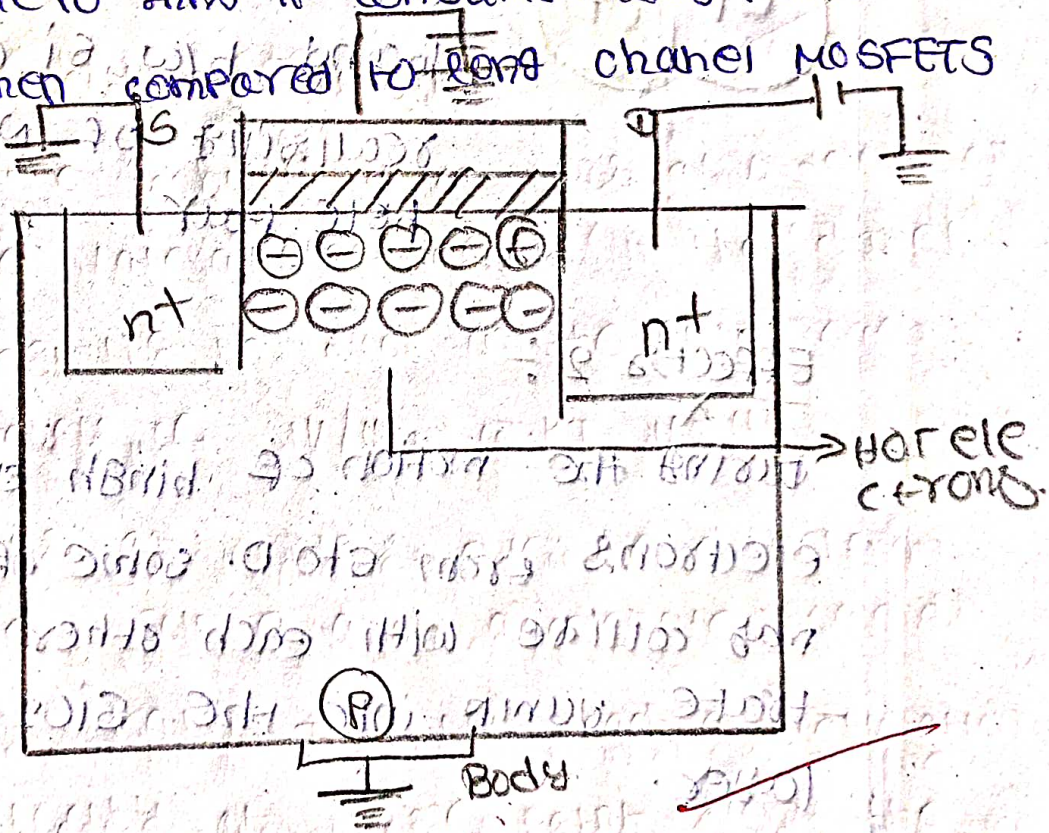
In short chanel MOSFET:

⇒ chanel length L is very small, and it is interms of "nano/meters"

ω·K·T E≥ VDS LL

here due to decrease in 'L' the lateral electric field E will be more than DIOS.

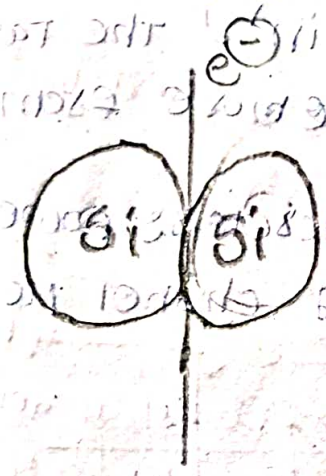
Due to this it consumes less power when compared to long chanel MOSFETS



Due to the application of High VDS at the D terminal in electrons will get more energetic these high energetic electrons are called as HOT electrons.

Effect ① :-

Impact Ionisation :- It is process in a material by which one energetic carrier can lose their energy by certain of another charge carrier.



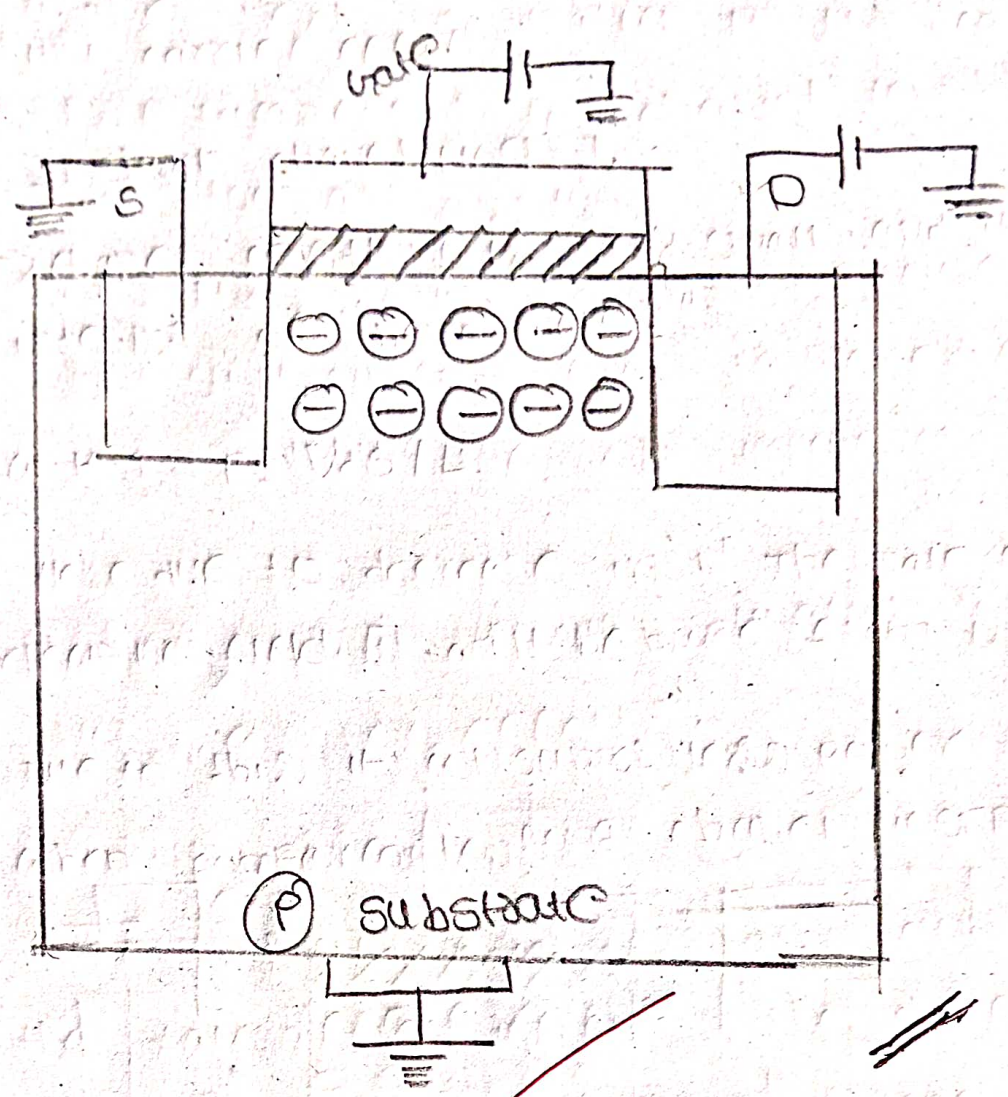
Here the high electric electron colliding the Si atoms & breaks the convalent band b/w Si atoms by realising of new electron hole pair.

Effects 2 :-

During the motion of high energetic electrons from S to D. some of them may collide with each other will penetrate jump into the SiO_2 oxide layer.

→ So here we get another flow of current which opposite to current in impact Ionisation (I_{IS}). this current is called as "trap current".

i.e I_g -


gate
S
D
P
substrate

R-19

College Code: 09

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NANDYAL-518501

IV B. Tech I-Semester- Mid-II *Examinations*

VLSI DESIGN

ECE

Max. Marks: 20 Date: 09-12-2022 Time: 2 Hours

Note: 1.Answer first question compulsorily. (5 x 1= 5 Marks)

2. Answer Any *THREE* from 2 to 5 questions.(3 x 5 = 15 Marks)

Q. No			M	CO	BL
Q.1	a)	Define sheet resistance.	1M	CO3	BL1
	b)	Define velocity saturation.	1M	CO4	BL1
	c)	Define DIBL.	1M	CO3	BL1
	d)	Define Hot-carriers.	1M	CO5	BL1
	e)	What is a glitch?	1M	CO4	BL2
Q.2	a)	Estimate the delay of CMOS inverter driven by another CMOS inverter.	3M	CO3	BL2
	b)	Estimate the delay of NMOS inverter driven by another NMOS inverter.	2M	CO3	BL2
Q.3	a)	Explain about different MOS device models.	3M	CO5	BL3
	b)	What are process corners? Explain in detail.	2M	CO5	BL3
Q.4	a)	Explain about VTCMOS and MTCMOS techniques.	3M	CO4	BL2
	b)	What are the various sources of power dissipation?	2M	CO4	BL2
Q.5	a)	Calculate the capacitance for the dimensions L=20λ, W=3λ to metal-1, polysilicon and n-type diffusion layers. (relative capacitance for metal 1 is 0.075, polysilicon is 0.1 and n-type diffusion is 0.25).	3M	CO3	BL2
	b)	Explain wiring capacitances.	2M	CO3	BL1

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VLSI Design

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Note: 1. Answer first question compulsorily. (5 x 1 = 5 Marks)

2. Answer Any *THREE* from 2 to 5 questions. (3 x 5 = 15 Marks)

Q.No			M	CO	BL
Q.1	a)	What are the advantages of CMOS over Bipolar technology	1M	CO1	BL1
	b)	Explain diffusion process in IC fabrication.	1M	CO1	BL2
	c)	What is pass transistors? Write merits and demerits of it.	1M	CO3	BL1
	d)	Explain the design rules for wires and contacts?	1M	CO2	BL2
	e)	What is stick diagram? Draw the stick symbols of MOS layers.	1M	CO2	BL3
Q.2	a)	Explain CMOS fabrication using N-well process with neat diagrams.	3M	CO1	BL2
	b)	Discuss about lithography and oxidation process	2M	CO1	BL1
Q.3	a)	Explain the transfer characteristics of CMOS inverter with neat sketch?	3M	CO1	BL3
	b)	Explain about Bi-CMOS inverters?	2M	CO3	BL2
Q.4	a)	Derive the MOSFET current equation in saturation region?	3M	CO1	BL3
	b)	Explain different alternative forms of nMOS inverter?	2M	CO3	BL2
Q.5	a)	Design a circuit and stick diagram of NOR gate?	3M	CO2	BL3
	b)	Design a layout of NOR gate?	2M	CO2	BL3

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RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING & TECHNOLOGY

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(ESTD-1995)

INTERNAL EXAMINATIONS ANSWER BOOKLET

Principal
Autonomous
RGEM

NAME OF THE STUDENT: C. Dhanush Kumar Reg. No. 1 9 0 9 1 A 0 4 3 5

	1	2	3	4	5
A	1	2½	✓	3	3
B	1	1½		2	2
C	1				
D	1				
E	1				
Total	5	4	2	5	5

Grand Total :(In Figures) 19

(in Words): One Nine.

NAME OF THE SUBJECT: VLSI Design

INTERNAL EXAM : I / II

Date of Exam: 09/11/22 (FN/AN)

Course : B.Tech. / M.Tech./ MBA / MCA

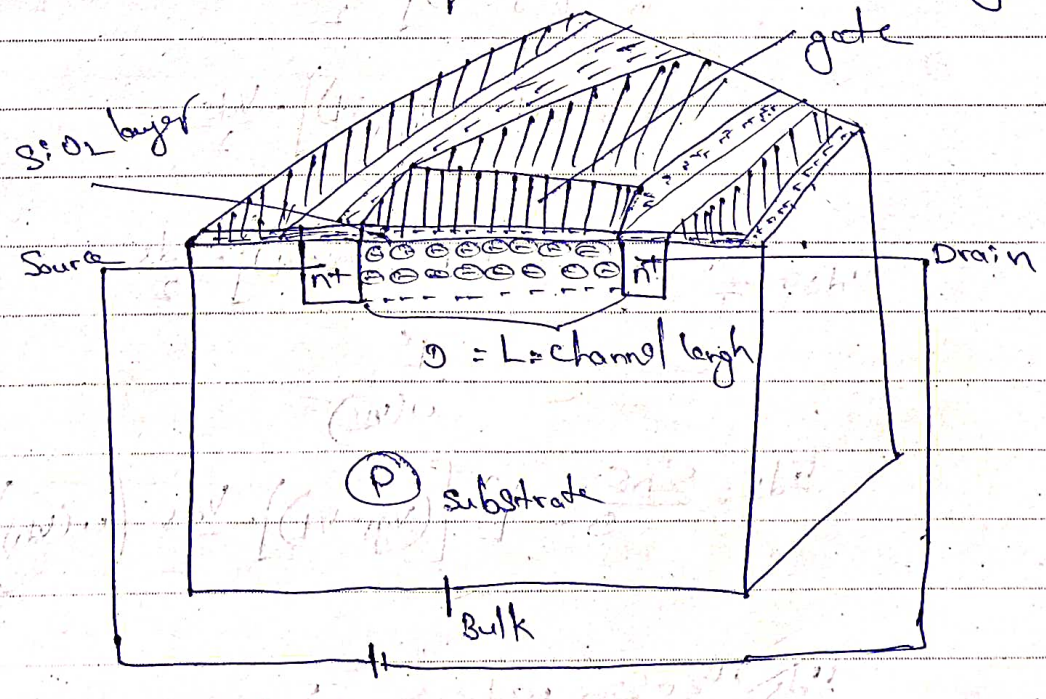
Year : IV Sem.: I

Branch: ECE

Signature of the Invigilator

(Start Writing From Here)

4a MOSFET current equation in Saturation region.



We know that $I = \frac{Q}{T}$

$I_{ds} = \frac{Q_c}{T}$

$$T = \frac{L}{V}$$

$$V = \mu E$$

$$E = \frac{V_{DS}}{L}$$

$$\therefore V = \mu\left(\frac{V_{DS}}{L}\right) \Rightarrow T = \frac{L}{\mu\left(\frac{V_{DS}}{L}\right)} = \frac{L^2}{\mu(V_{DS})}$$

$$\boxed{Q_C = \frac{\varepsilon_0 \varepsilon_{in} E_g}{D}}$$

$$E_g = \left[(V_{gs} - V_t)\right] - \frac{V_{DS}}{2}$$

$$Q_C = \frac{\varepsilon_0 \varepsilon_{in} E_g w.L}{D} \quad \text{for NMOS}$$

$$Q_C = \frac{\varepsilon_0 \varepsilon_{in} E_g . w L}{D}$$

$$= \frac{\varepsilon_0 \varepsilon_{in}}{D}\left[(V_{gs} - V_t)\right] - \frac{V_{DS}}{2} . w . L$$

$$= \frac{\varepsilon_0 \varepsilon_{in} . w L}{D}\left[(V_{gs} - V_t)\right] - \frac{V_{DS}}{2}$$

$$I_{DS} = \frac{Q_C}{T} = \frac{\frac{\varepsilon_0 \varepsilon_{in} w . L}{D}\left[(V_{gs} - V_t)\right] - \frac{V_{DS}}{2}}{\frac{L^2}{\mu(V_{DS})}}$$

$$I_{DS} = \frac{\varepsilon_0 \varepsilon_{in}}{D} \cdot \frac{w}{L}\left[(V_{gs} - V_t)\right] - \frac{V_{DS}}{2}\left(\mu(V_{DS})\right)$$

$$I_{DS} = \frac{\mu \varepsilon_0 \varepsilon_{in}}{D} \cdot \frac{w}{L}\left[(V_{gs} - V_t)\right] V_{DS} - \frac{V_{DS}^2}{2}$$

∴ This is the Source to drain current equation in Linear region.

Current equation is saturation region

$$(V_{gs} - V_t) \leq V_{ds} \Rightarrow (V_{gs} - V_t) = V_{ds}$$

$$I_{ds} = \frac{\mu \varepsilon_0 \varepsilon_{in}}{D} \cdot \frac{W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

$$I_{ds} = \frac{\mu \varepsilon_0 C_{in}}{D} \cdot \frac{W}{L} \left[V_{gs}^2 - \frac{V_{ds}^2}{2} \right]$$

$$I_{ds} = \frac{\mu \varepsilon_0 \varepsilon_{in}}{D} \cdot \frac{W}{L} \left[\frac{V_{ds}^2}{2} \right]$$

Let $\frac{\mu \varepsilon_0 C_{in}}{D} = k$

$$I_{ds} = \frac{\mu \varepsilon_0 \varepsilon_{in}}{D} \cdot \frac{W}{L} \left[\frac{V_{ds}^2}{2} \right]$$

$$I_{ds} = k \cdot \frac{W}{L} \left[\frac{V_{ds}^2}{2} \right]$$

Let $\beta = k \cdot \frac{W}{L}$

$$I_{ds} = \beta \left[\frac{V_{ds}^2}{2} \right]$$

3

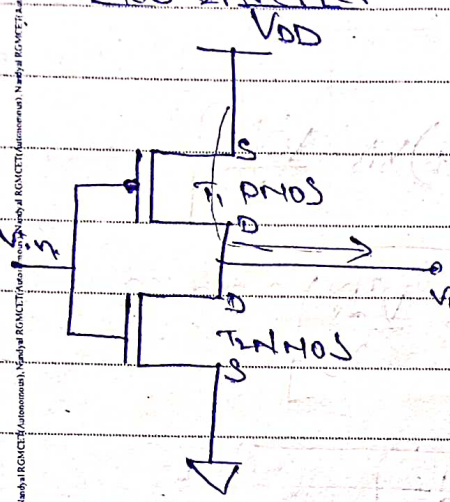
the current equation in the saturation region

$$I_{ds} = \frac{\mu \varepsilon_0 C_{in}}{D} \cdot \frac{W}{L} \left[\frac{(V_{gs})^2}{2} \right]$$

4b. Different alternative forms of NMOS Inverter

CMOS :- It is the combination of NMOS and PMOS transistors

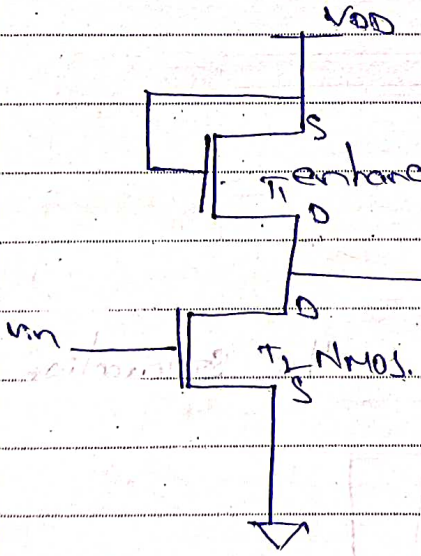
CMOS Inverter



for Logic '0'
T_1 is ON
T_2 is OFF

for Logic '1'
T_1 is OFF
T_2 is ON

Enhancement NMOS Inverter :- By replacing the PMOS transister with the enhancement NMOS transistor is called the enhancement NMOS Inverter.



⇒ In the enhancement NMOS ~~and~~ inverter we can connect the enhancement NMOS transistor inverter

in the place of PMOS transistor. so, the circuit size of the inverter is less (small).

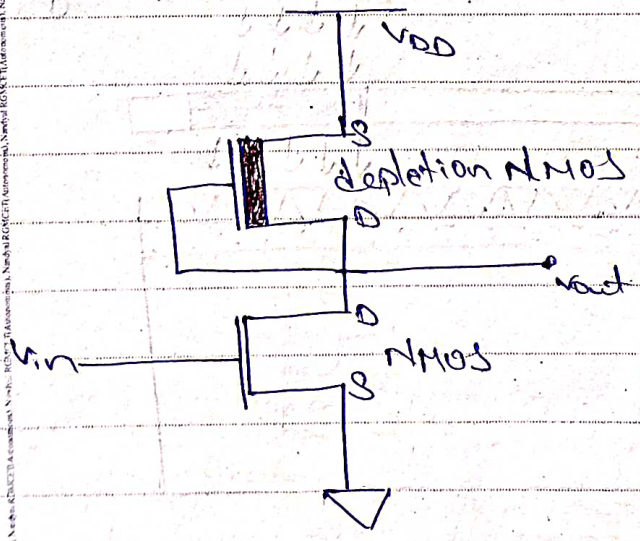
Advantages

=> Circuit size is decreases
=> less space occupies.
=> high current gain capability.

Disadvantages

=> Due to enhancement NMOS transister the circuit is always ON.
=> the power consumption is high
=> It will not gives the full swing current (zero current).

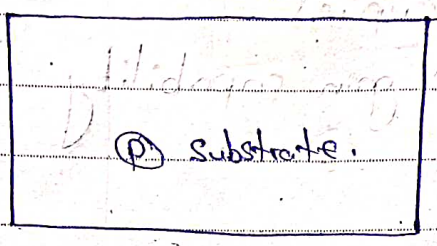
Depletion NMOS Inverter :- By replacing the PMOS trasistor with the depletion NMOS transistor is called depletion NMOS Inverter.



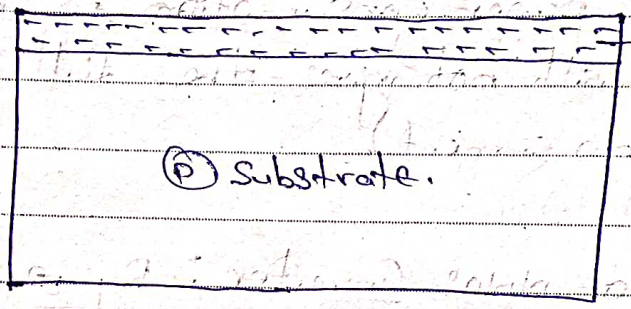
=> Advantages
=> It gives the full swing current
=> consumes power descipition is low.

2a. CMOS fabrication using N-well process with neat diagram.

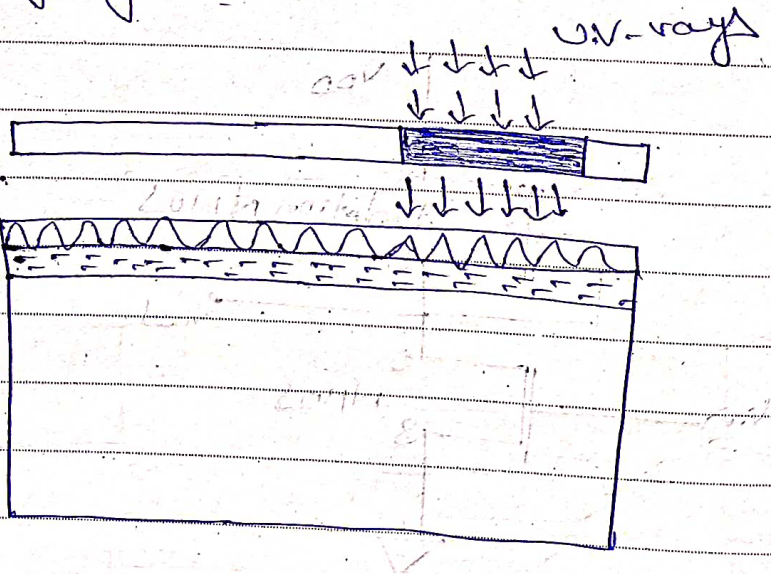
① Prepation of p-type Substrate.



② oxidation process :- formation of thin oxide layer on the top of the p-Substrate

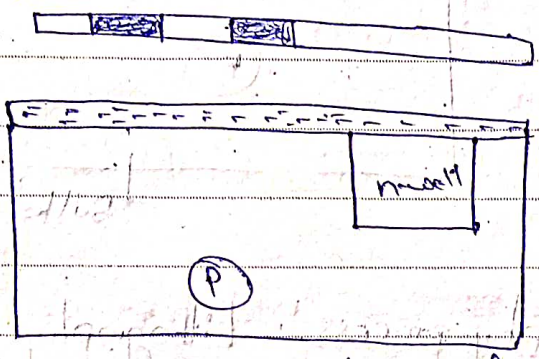


③ photolythography process.

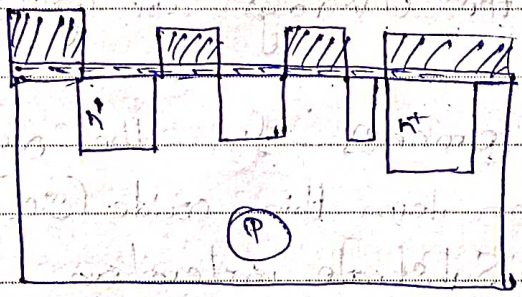


⇒ In the photolythography process the UV rays will falls on the substrate and forms the n-well

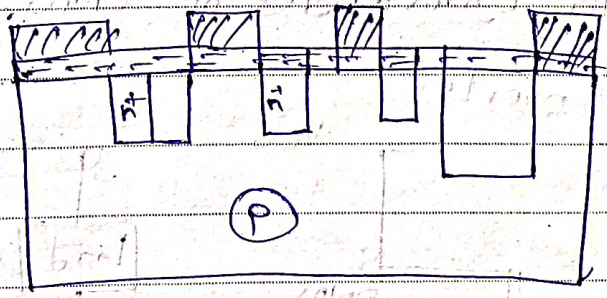
Etching process



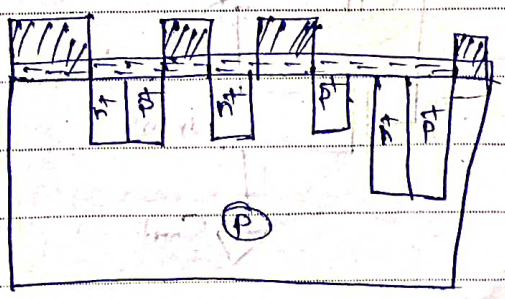
3) Formation of gate terminal and pattern silicon.



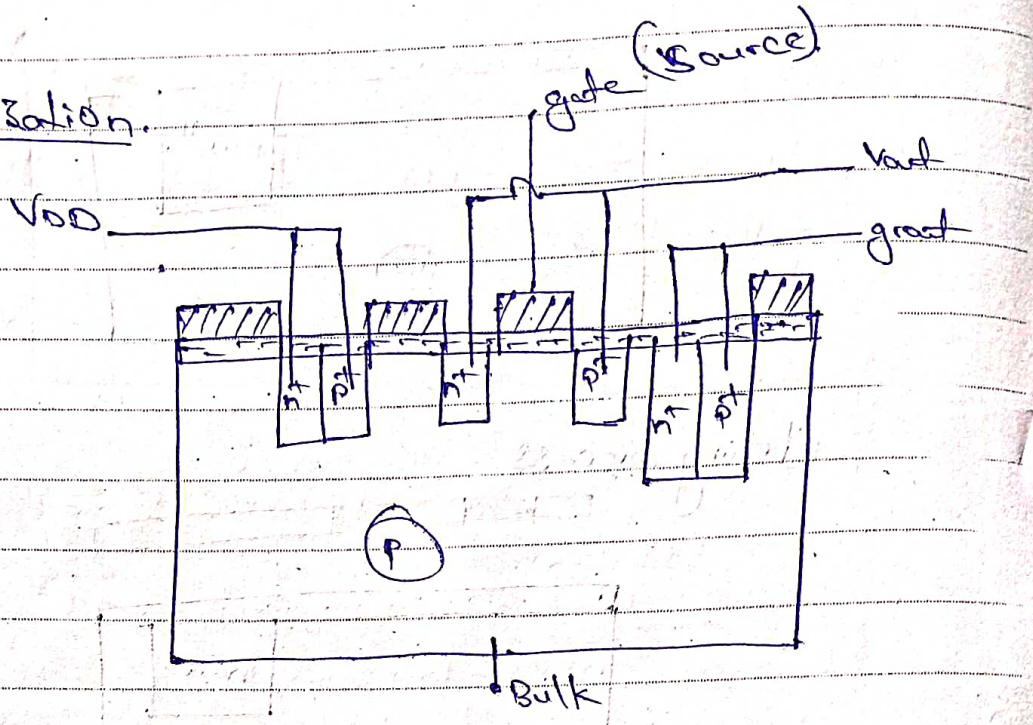
4) n^+ diffusion



5) p^+ diffusion.



Metalization.

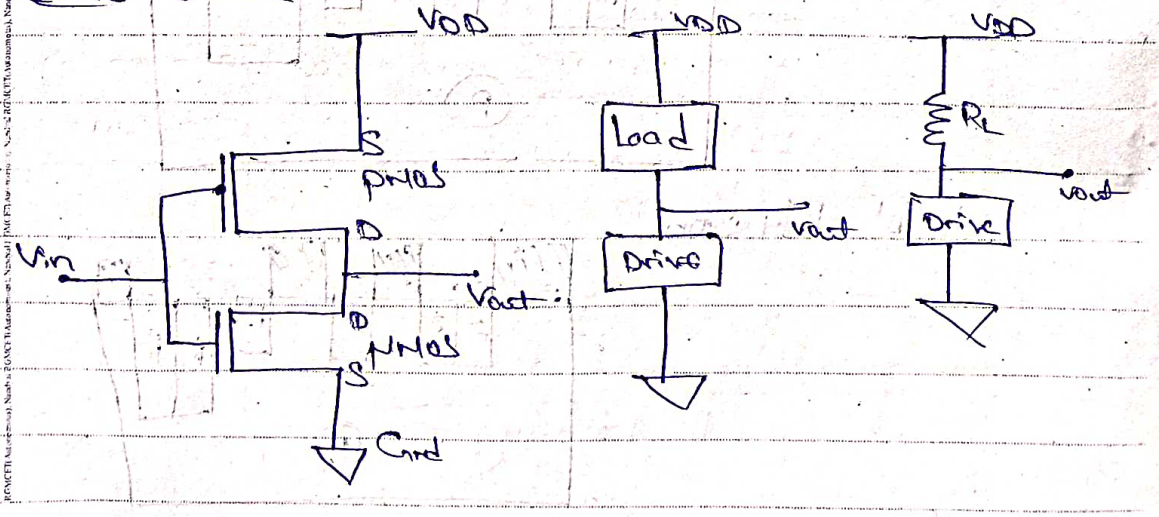


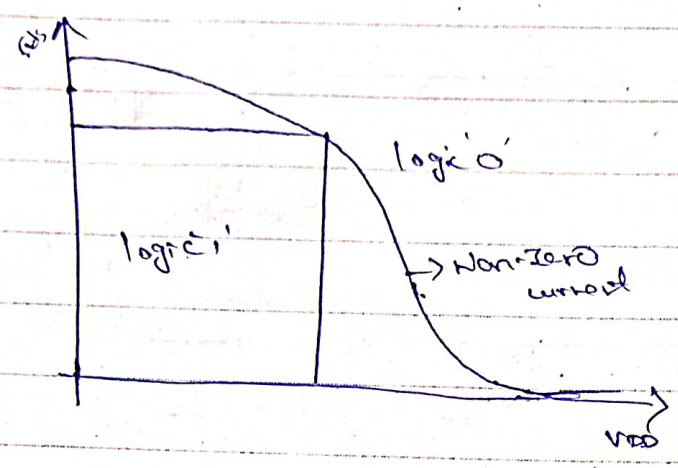
2b. Lithography process :- Lithography is the process in which we have to remove the unwanted part by using the U.V-rays (sun-light)

4. Oxidation process :- In the oxidation process the we can form thin oxide (SiO_2) layer on the top of Substrate ~~material~~ material and ~~also~~ p-diffusion and n-diffusion.

3a. Transfer characteristics of CMOS inverter.

CMOS Inverter





for logic '0' → PMOS - ON - NMOS - OFF
for Logic '1' → NMOS - ON - PMOS - OFF

1a. Advantages of CMOS over Bipolar.
⇒ Low power description
⇒ high current probability
⇒ low cost
⇒ Circuit design is easy.

b. Diffusion process in IC fabrication:- Adding of 5v (or) 3v group impurities (p^+ or n^+ ions) into the substrate is called the diffusion process.

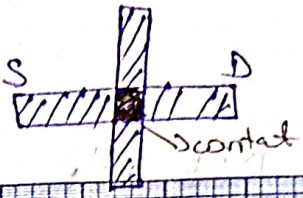
c. Pass transister:- The transister which pass the output values from one node to another node is called the pass-transister.

Merites	Demerits
⇒ low cost	⇒ It give full swing current
⇒ low power description	⇒ not give zero current

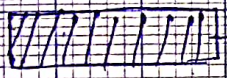
(1d) design rules for wires and contacts.

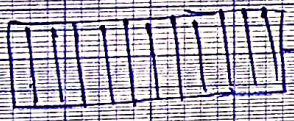
→ for wires vertical lines represents

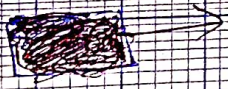
→ for contact black part represent.

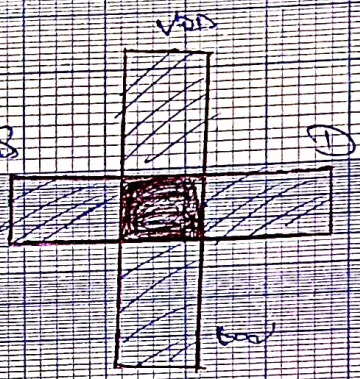


(1e) Stick diagram :- The layout (or) blue print of the circuit diagram with the internal connections is called the stick diagram.





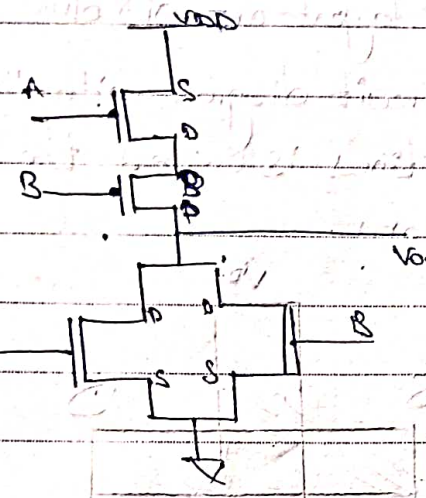




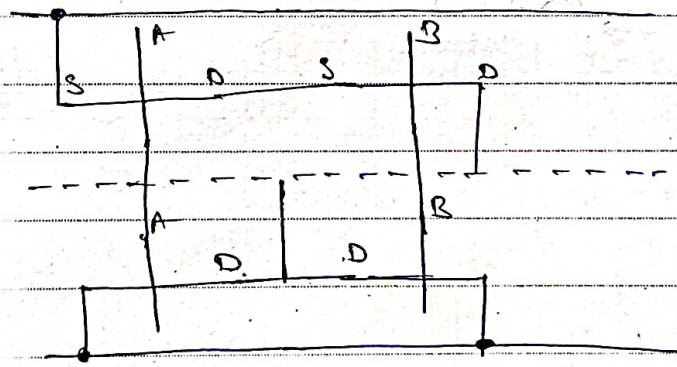
5a. NOR gate

$Y = \overline{A+B}$

Circuit diagram

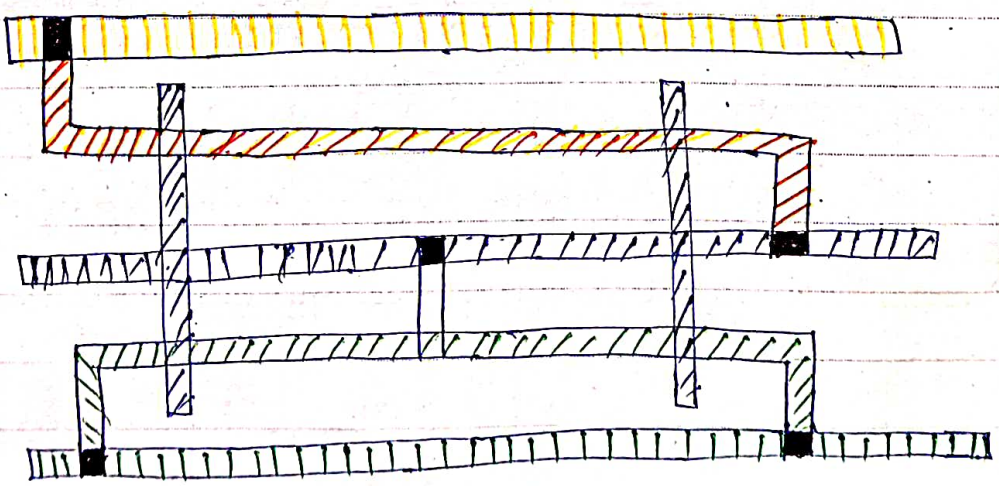


Stick-diagram



3

5b. layout-diagram



S.No. 50023

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING & TECHNOLOGY

AUTONOMOUS

Accredited by NAAC of UGC, New Delhi with 'A' Grade:: Accredited by NBA
Affiliated to JNT University Anantapur
Nandyal - 518 501, Kurnool Dist, A.P.

(ESTD-1995)

Principal
RGMCET Autonomous
NANDYAL

INTERNAL EXAMINATIONS ANSWER BOOKLET

NAME OF THE STUDENT: Shaik Farhan Reg. No. 1 9 0 9 1 A 0 4 3 9

	1	2	3	4	5
A	1	1		3	3
B	1	1		2	2
C	0				
D	1				
E	1				
Total	4	2		5	5
Grand Total :(In Figures)	16				
(in Words):	One Six.				

NAME OF THE SUBJECT: VLSI Design

INTERNAL EXAM : I / II

Date of Exam: 9/12/2022 (FN/AN)

Course : B.Tech. / M.Tech./ MBA / MCA

Year : IV Sem.: I

Branch: ECE

Signature of the Invigilator

(Start Writing From Here)

1) a) Sheet resistance:-

The resistance present between the 2 ends of a sheet is called sheet resistance.

It is given by Ω/R_s, It differs from material to material.

1) b) Velocity saturation:-

In designing low power circuits we vary the threshold voltages due to which the speed of the device increases. The velocity of electrons also increases. But after certain speed the velocity reaches to saturation.

This process is called velocity saturation.

1) c) DIBL

It refers that on providing digital input we obtain

binary output. Such logics are called DIBL.

1) d) Hot carriers:-

In scaling of MOSFET process we convert long channel mosfet to short channel mosfet.

In this process channel length L decreases which inturn increases the energy. Due to more energy some of electrons gain high power and their mobility is very high. Such are called hot carriers.

1) e) Glitch

→ The unwanted noise or disturbance in the channel is called glitch.

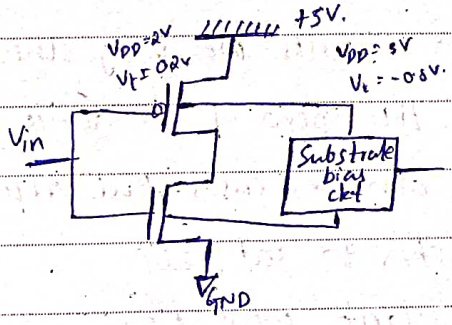
→ Due to glitches the original information is transmitted with distortion and loss of information occurs.

4) a) In voltage scaling we vary the threshold voltage (V_t)

To perform this process we mainly follow 2 methods.

i) VTCMOS ii) MTCMOS.

i) VTCMOS (Variable threshold CMOS).



→ In variable threshold CMOS we vary the threshold voltage & V_{DD} to obtain different inputs.

→ By which we can increase the speed and avoid

sub threshold leakage current.

Advantages

i) High speed due to low V_{DD}.

ii) No sub threshold leakage current due to low V_t.

iii) Consumes less power.

iv) Heat dispation is less.

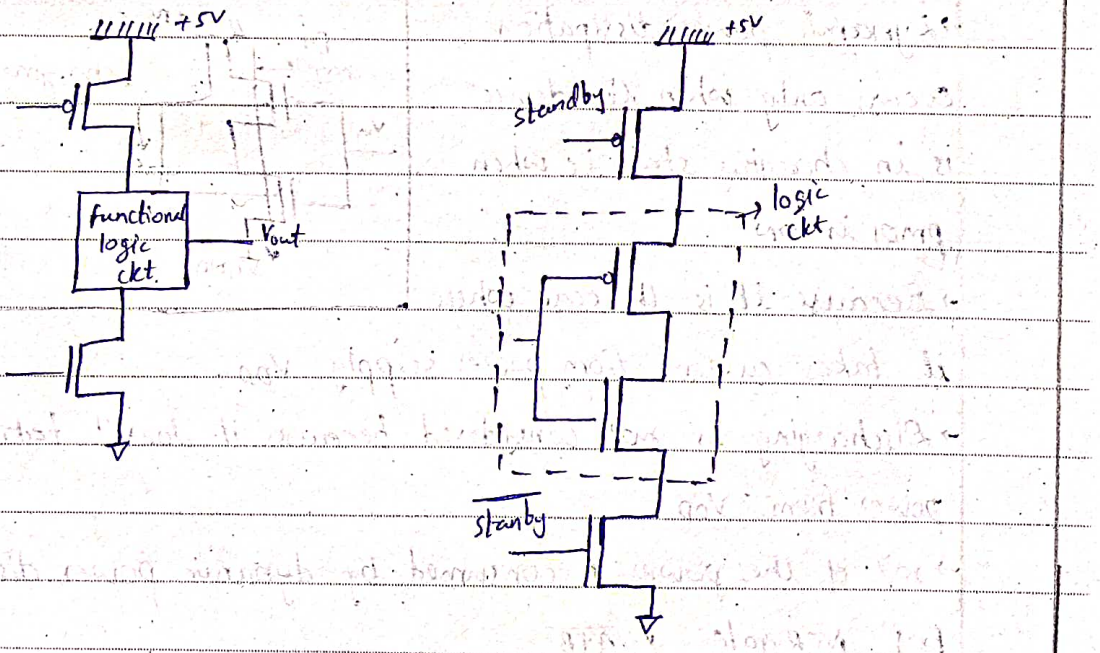
Disadvantages

i) Complexity increas as we've to implement substrate bias circuit.

ii) We must provide different V_{DD} which becomes difficult.

iii) Size of the circuit increases and becomes difficult to design.

ii) MTCMOS (Multiple Threshold CMOS)



Here we provide multiple threshold voltages for high speed and to avoid sub threshold leakage current. Rather than using various V_{DD} we use multiple threshold voltages to reduce complexity.

Advantages

i) High speed due to low V_{DD}

ii) No sub threshold leakage current.

iii) Easy to design and implement.

iv) Less complex.

Disadvantages

i) The number of transistors in a circuit increases.

---

4) b) There are mainly 3 sources of power dissipation.

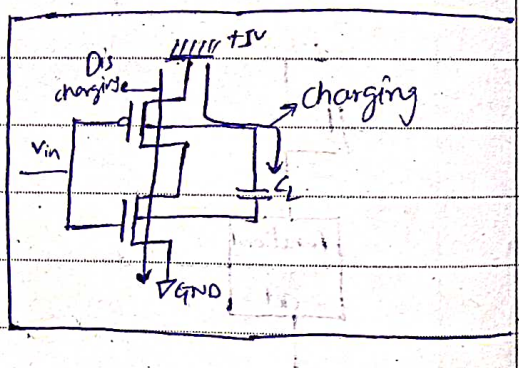
i) Dynamic power dissipation.

ii) Short circuit power dissipation

iii) Leakage power dissipation.

i) Dynamic power dissipation:-

→ Dynamic power dissipation occurs only when the device is in charging state i.e when pmos is ON.

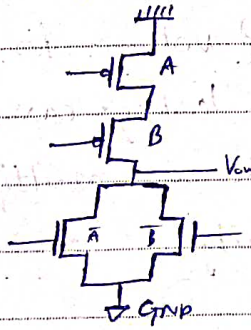


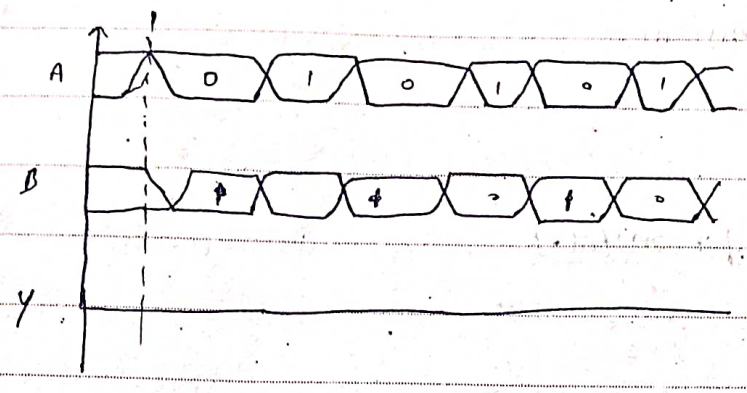
→ Because it is the case where it takes current from power supply V_{DD}.

→ Discharging is not considered because it doesn't take power from V_{DD}.

→ 50% of the power is consumed by dynamic power dissipation

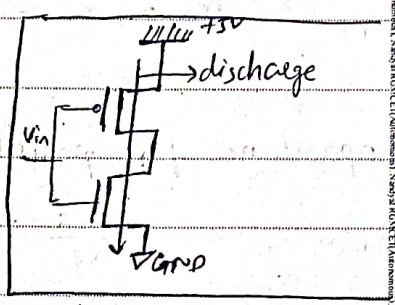
Ex:-) NOR gate. $Y = \overline{A+B}$





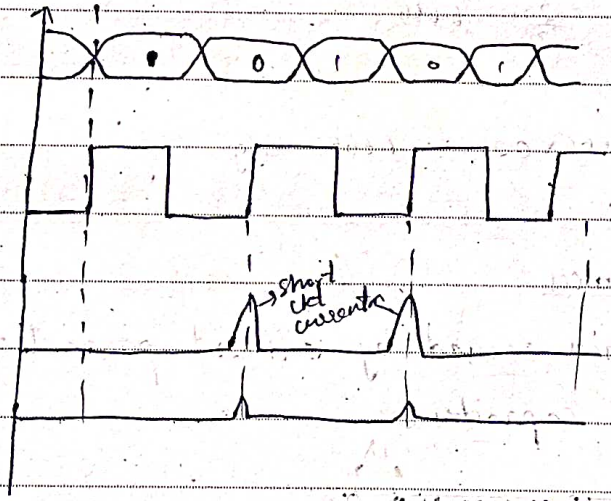
ii) Short circuit power dissipation

→ Short circuit power dissipation occurs in the case where both the transistors (pmos, nmos) are in ON state.



→ The total power discharges to the ground.

→ No power will be obtained at the output side.



iii) Leakage power dissipation

→ Leakage power dissipation occurs whenever the device is OFF state still the power is flowing in the device.

→ Such case is called leakage power dissipation.

→ There are 2 types of leakage power dissipations.

i) Diode reverse leakage current.

ii) Sub-threshold leakage current.

5) a) Given dimensions.

$L = 20\lambda$

$W = 3\lambda$

Capacitance for metal-1

$$z = \frac{20 \times 3}{2 \times 2} = 15$$

$$= 15 \times 0.075 = 1.125 \square Cg.$$

Capacitance for polysilicon.

$$= \frac{6 \times 6}{3 \times 3} = 2.4$$

$$= .4 \times 0.1 = 0.4 \square Cg.$$

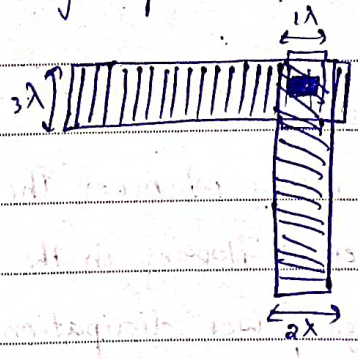
Capacitance for n-type

$$= \frac{20}{3} = 6.666$$

$$= 6.666 \times 0.25 = 1.6666 \square Cg.$$

5) b) Wiring capacitances

→ The capacitances caused by different parameters are called wiring capacitances.



There are 3 types of wiring capacitances

i) fringing capacitance.

ii) relative capacitance.

iii) sheet capacitance.

i) fringing capacitance:-

→ The capacitance caused by fringe is called fringe capacitance.

→ The different lengths while adding up cause fringes.

ii) Relative capacitance:-

→ The relative capacitance depends on the material

→ Different materials consist of different relative capacitances.

Sheet capacitance.

→ The capacitance caused by sheet or present in the sheet.

→ The capacitance present in between 2 ends of sheet is called sheet capacitance.

2) a) Estimation of delay of cmos inverter driven by another cmos inverter.

i) XOR gate

Truth table

A	B	Y	
0	0	1	1/4
0	1	0	1/4
1	0	0	
1	1	1	

$= P_0 \times P_1 = \frac{1}{4} \times \frac{1}{4} = \frac{1}{8}$

ii) XNOR ⇒

A	B	Y	
0	0	0	3/4
0	1	1/2	
1	0	1	
1	1	1	

$= \frac{3}{4} \times \frac{1}{4} = \frac{3}{16}$

NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

3/4

$= \frac{3}{4} \times \frac{1}{4} = \frac{3}{16}$

NOR gate.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$\frac{1}{4} \times \frac{3}{4} = \frac{3}{16}$

2. b) Estimation delay of nmos inverter driven by another nmos.

AND gate

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

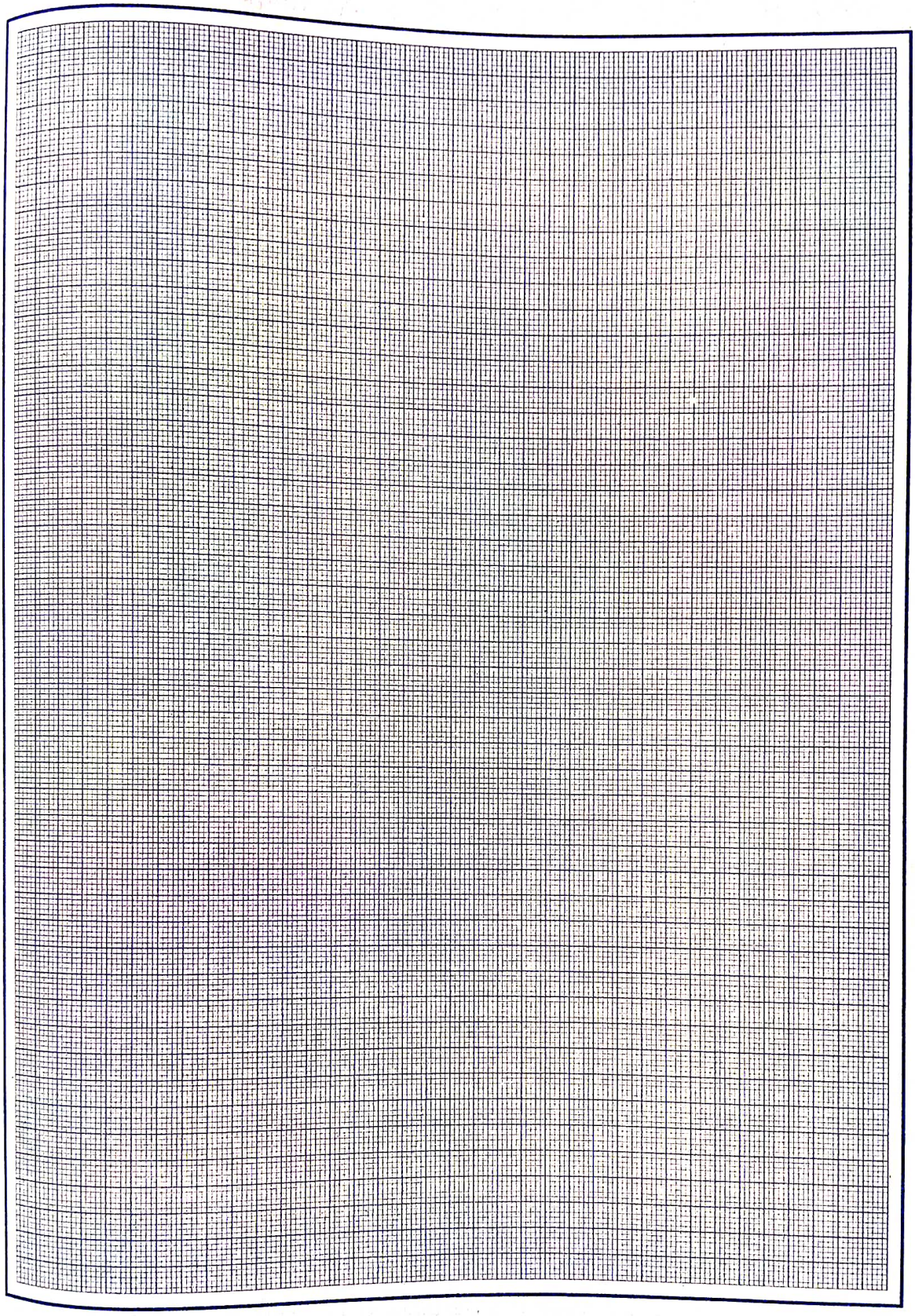
3/4

$= \frac{3}{4} \times \frac{1}{4} = \frac{3}{16}$

OR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

$\frac{3}{4} \times \frac{1}{4} = \frac{3}{16}$



Code: A0426197R1222

RGM COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

23rd December 2022

IV B.Tech. I Sem. (R19) End Examinations (Regular)

VLSI DESIGN

ECE

Time: 3 Hrs **Total Marks: 70**

Note 1:Answer Question No.1 (Compulsory) and 4 from the remaining

2:All Questions Carry Equal Marks

1a	Draw the Bi-CMOS inverter with no static current flow and give its advantages.	
b	What are the main steps involved in typical n-well process?	
c	Define fringing fields.	
d	What is threshold voltage?	
e	What is transistor sizing?	
f	What are the CMOS λ-based design rules?	
g	What is the body effect and explain?	
2	a) What is voltage scaling? How will you reduce the power using voltage scaling?	(7)
	b) Explain the concept of MTCMOS techniques.	(7)
3	a) Calculate resistance for NMOS and CMOS inverters.	(7)
	b) Calculate delay of two stage CMOS inverters.	(7)
4	a) Write about analog design in digital world.	(7)
	b) Explain about charge and capacitance modelling.	(7)
5	a) Draw the CMOS physical structure.	(4)
	b) Explain p-well process in CMOS fabrication in detail with neat diagrams.	(10)
6	Draw the stick diagram and layout for	
	a) NMOS inverter.	(7)
	b) P-Well CMOS inverter.	(7)
7	Derive the expression for following	
	a) Trance conductance g_m	(5)
	b) Output conductance g_{ds}	(5)
	c) Threshold Voltage V_t	(4)

- xxx -

Code: A042b197R1222

RGM College of Engineering & Technology
(Autonomous)

(1)

IV B.Tech. I-Semester (R-19) End Examinations
(Regular)

VLSI Design

ECE

KEY.

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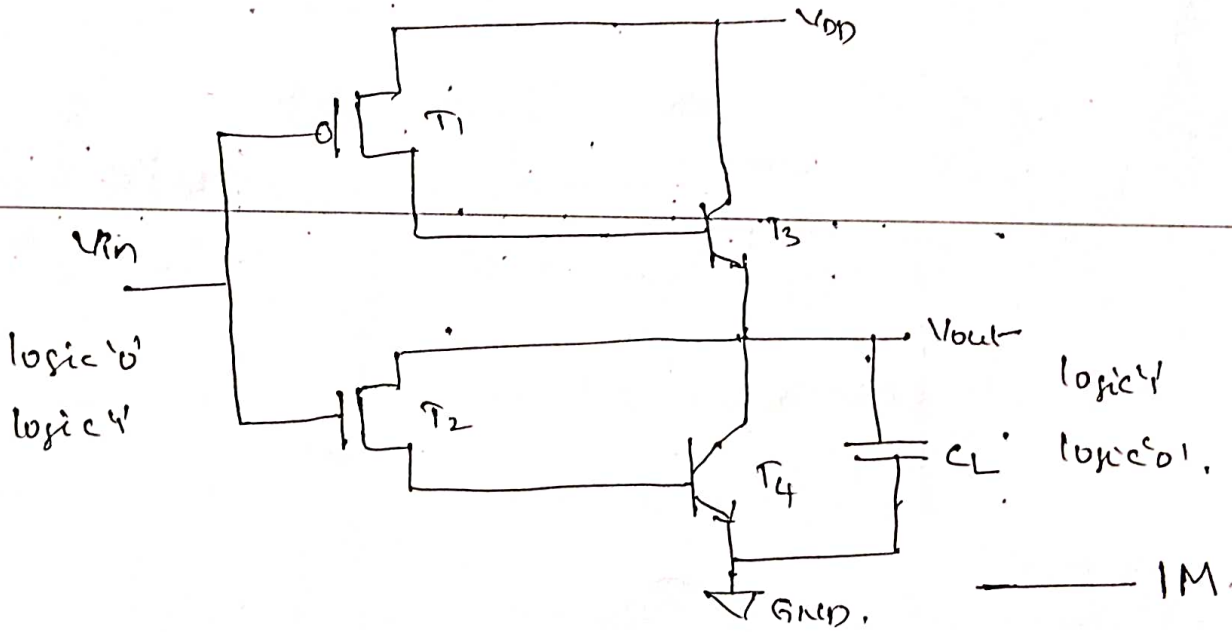
(1)(A)

Bicmos Inverter:

Bicmos Inverter is a combination of Bipolar Technology and cmos Technology.



1M

advantages:

- Input Impedance is high
- High output current
- Driving capability High
- voltage levels are good
- Static current flows, does not flows between power rails.

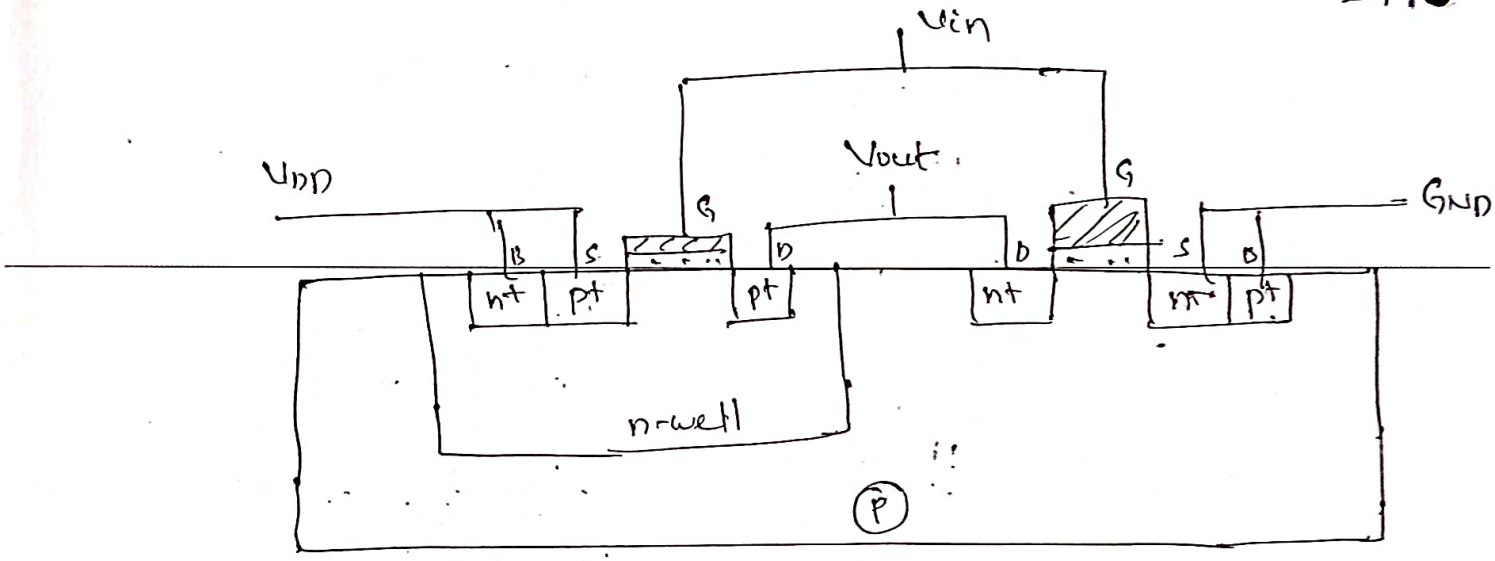
1M

(1) (B)

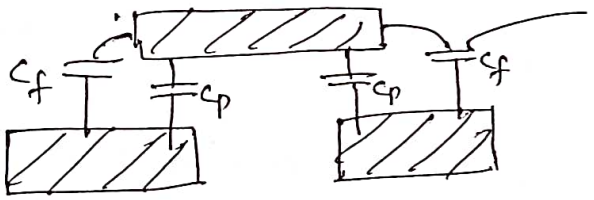
Main steps in CMOS fabrication using n-well process

1. Take p-type substrate
2. form the oxidation layer on Top of p-type substrate
3. Create a n-well with 4 μm to 5 μm depths.
4. do the diffusion process using p+ and n+ masks
5. metallization process

— 2M



(1) (C)



- Fringing field is a non-uniform field that appears near the edge of the plates. The capacitance occure due to this fringing field is called the fringing field capacitance. — 2M

(1) (d). Threshold Voltage:

Switching an enhancement mode mos transistor from the OFF to ON state consists in applying sufficient gate voltage to neutralize these charges and enable the underlying silicon to undergo an inversion layer due to the electric field from the gate.

$$V_t = \phi_{ms} \frac{Q_B - Q_{ss}}{C_0} + 2\phi_{fN}$$

Q_B = Charge per unit area

Q_{ss} = Charge density at Si : SiO_2 interface

C_0 = Capacitance per unit gate area

ϕ_{ms} = work function difference between gate and Si

ϕ_{fN} = Fermi level potential between inverted surface and bulk Si. —— 2M

(1) (e)

- Transistor sizing means reducing the dimensions of Transistor. (Lengths, Widths, oxide thickness - etc).
- Transistor channel length represents the Technology. it is represented as $L = 2\lambda$.
- Cant change the channel length randomly because it is technology dependent parameter.
- all other parameters are changes based the scaling factors. —— 2M

(1) (f) - λ- Based design rules are used to design the proper layout in VLSI

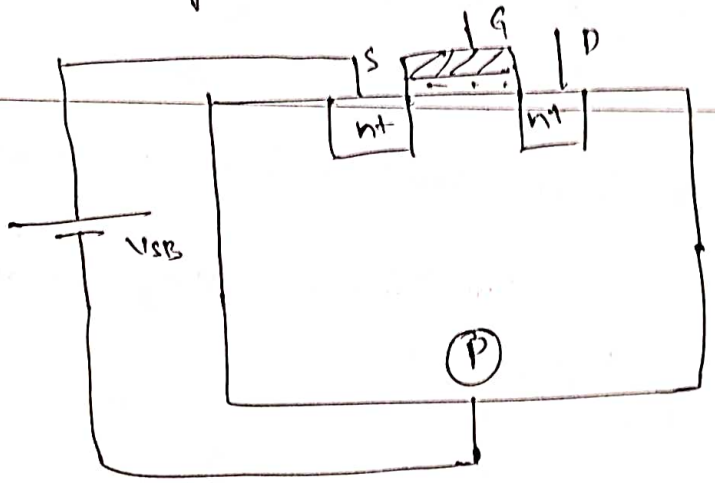
- These rules allow the scaling of complete wafer implementation

Ex: minimum metal width — 3λ

minimum metal spacing — 3λ. — 2M

(1) (g). Body effect:

The Body effect may also be taken into account since the substrate may be biased with respect to the source.



- increase the V_{SB} causes the channel to be depleted of charge carriers and thus the threshold voltage is raised. — 2M

- For change in V_t $\Delta V_t = \gamma (V_{SB})^{1/2}$

- For more lightly doped the substrate, the smaller will be the body effect.

(2) (A)

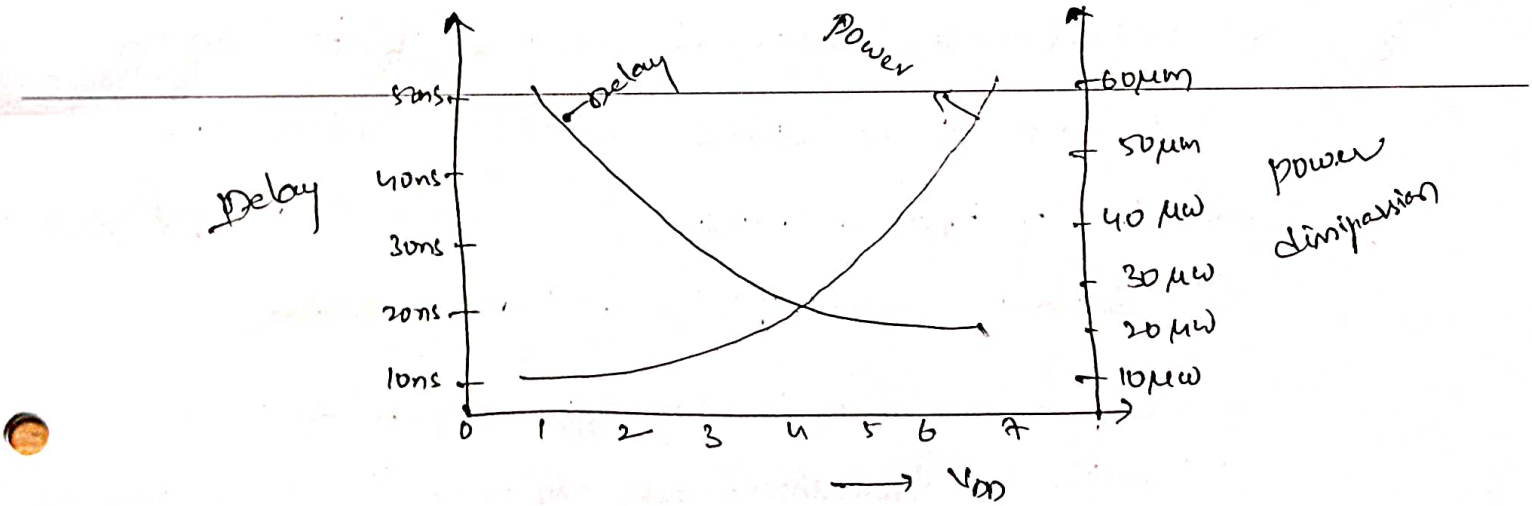
Voltage Scaling: Voltage scaling is a reduction of supply voltage (V_{DD}).

- Supply voltage is proportional to dynamic power dissipation

$$P_{dyn} \propto V_{DD}^2$$

- By doing voltage scaling or reduction of the supply voltage, dynamic power dissipation can be reduced.

$$P_{dyn} = \alpha_T \, C_L \, V_{DD}^2 \, f_{clk}.$$



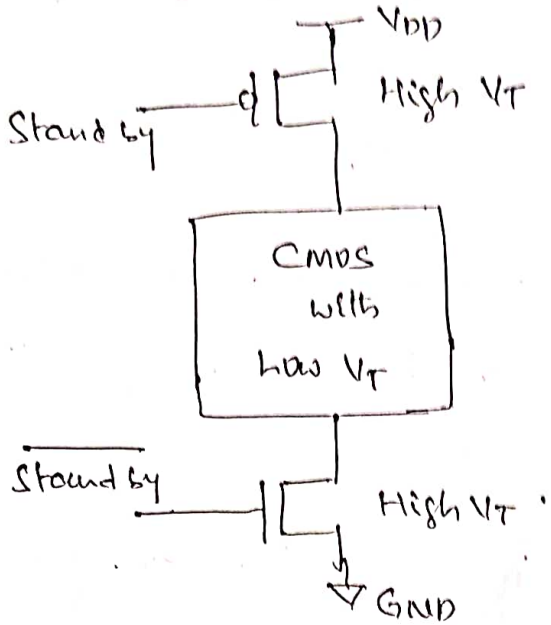
→ Reducing the supply voltage decrease the dynamic power. but time delay increases.

- To compensate or decrease time delay, decrease the threshold voltage of the device so that we can achieve both low power and improved speed performance.

— JM

(Q)(B) MTCMOS Technique :

- multiple threshold CMOS Technique having different threshold transistors.

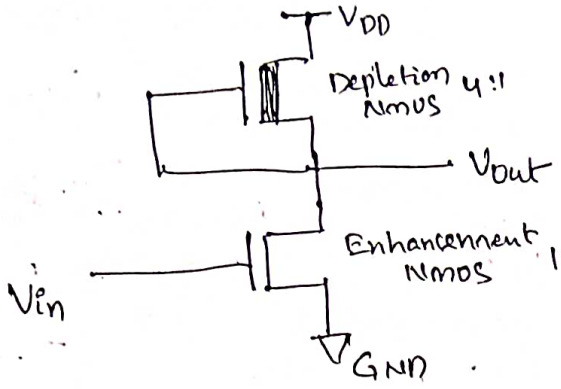


— 4M

- actual logic design is designed with Low V_T transistors to avoid switching time delay.
- Supply voltage reduced to 2V from 5V so that dynamic power dissipation ~~not~~ decreases.
- when circuit is in operating mode both High V_T transistors are ON and it is connected to power rails.
- → when circuit in stand by mode, High V_T transistors are get off and it is disconnected from the power rails so that Subthreshold leakage current can be reduced. — 3M
- → Here no need to use the substrate bias circuit to control the threshold voltage of transistors.

(3) (A) NMOS Inverter:

(4)



$$Z_{pu} = \frac{L_{pu}}{W_{pu}}$$

$$Z_{pd} = \frac{L_{pd}}{W_{pd}}$$

ON Resistance of pullup Transistor $R_{ON} = 2R_s$

$= 4 \times 10^4$

$= 40k\Omega$.

ON Resistance of pulldown Transistor $R_{ON} = Z.R_s$

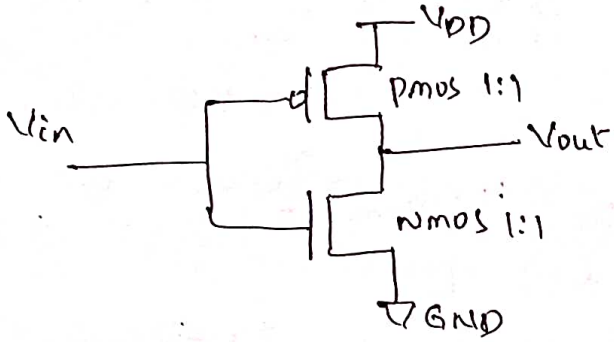
$= 1 \times 10^4$

$= 10k\Omega$

Total $R_{ON} = 40k\Omega + 10k\Omega = 50k\Omega$.

—— 4M

CMOS Inverter:



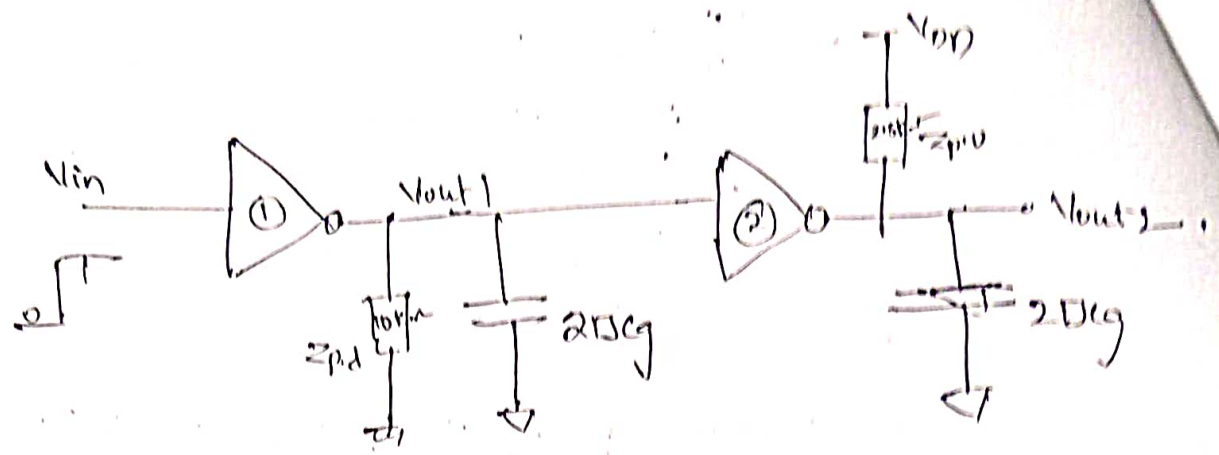
For pmos — $R_{ON} = 1 \times 2.5 \times 10^4 = 25k\Omega$

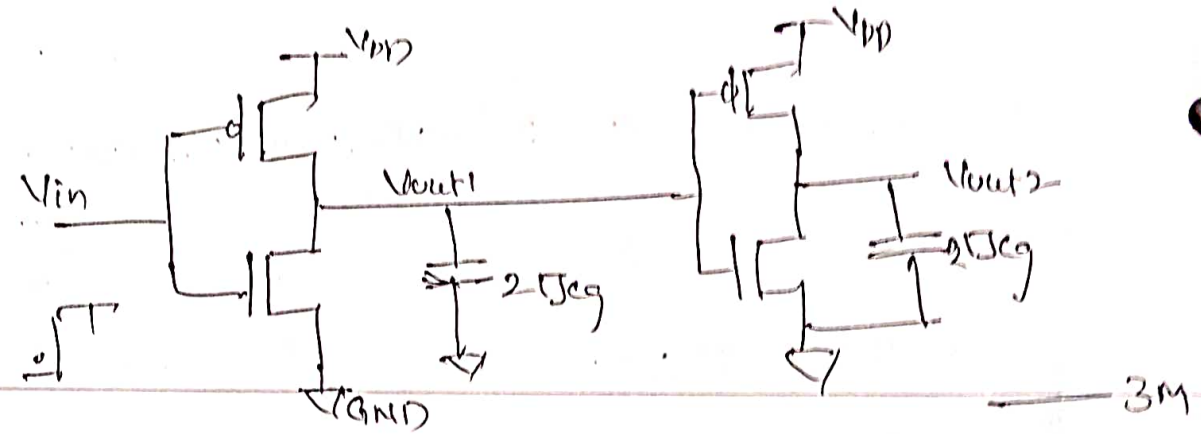
Nmos — $R_{ON} = 1 \times 10^4 = 10k\Omega$.

For CMOS, ON Resistance can be calculated individu transistors only.

—— 3M

(3) (B). Delay of an Two stage CMOS Inverter:





— 3M

For Stage ①: Delay time = $1R_s \times 2C_{eq}$

$= 2\tau$.

For Stage ②: Delay time = $2.5R_s \times 2C_{eq}$

$= 5\tau$.

Total Delay Time = Stage ① + Stage ②

$= 2\tau + 5\tau$

$= 7\tau$.

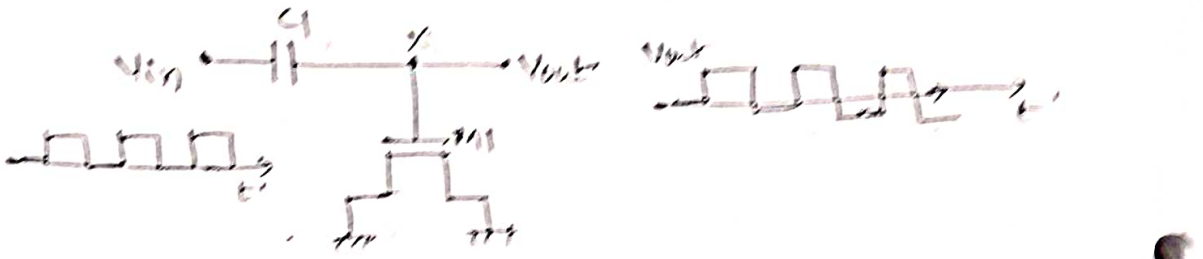
— 4M

(A) (A). — Memories and processors constitute the major major portion of today's semiconductor business.

- Most CMOS Technologies are designed, optimized and characterized for digital Applications.
- Despite the increasing emphasis on the "analog" accuracy of device models, we are still far from a point where we can fully trust the absolute numbers obtained in circuit simulations.
- Analog designers routinely encounter discrepancies in spice. For example, between ac analysis and transient analysis.
- Moreover, many device models fail simple benchmark tests and effects such as flicker noise and mismatch require measured data before they can be accurately reflected in simulations.
- The device models extracted from a wafer often fail to accurately predict the speed of the circuits fabricated on the same wafer.
- Under these conditions, Analog design relies on experience, intuition and measured data.
- The design of complex, high performance analog circuits may require data points that can be obtained only by first fabricating and characterizing many simpler test circuits.

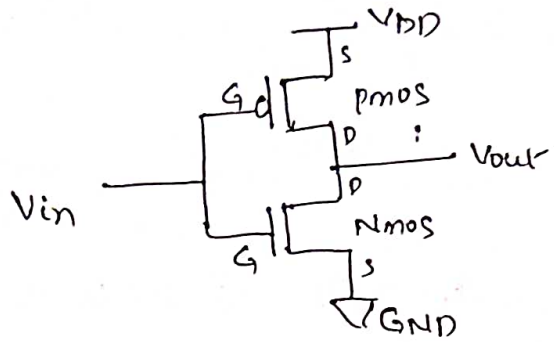
— TM

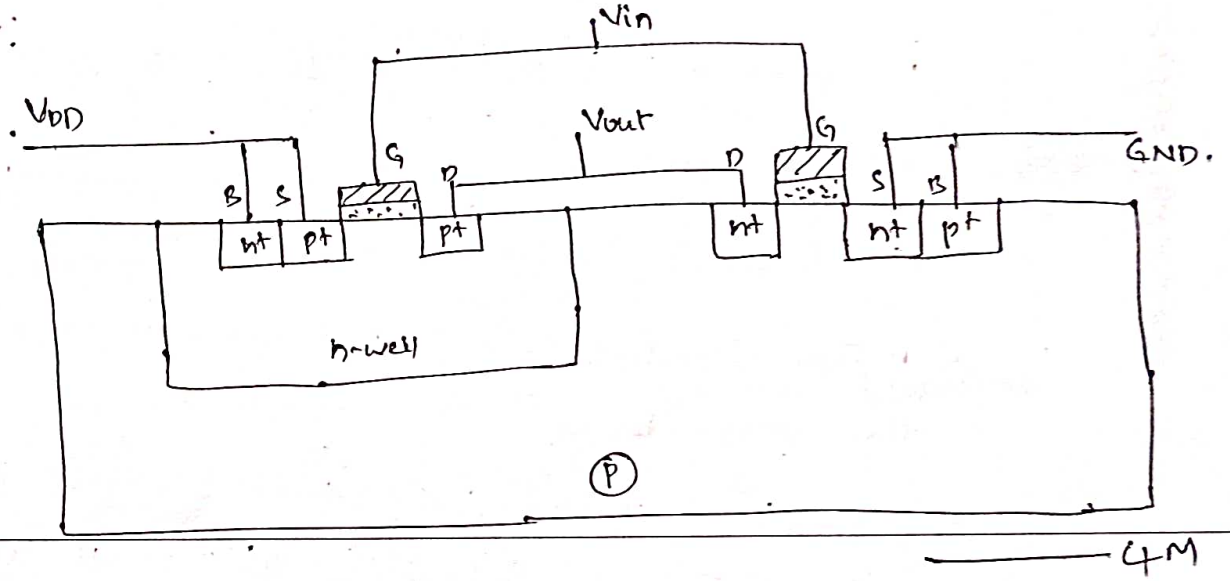
The simple gm capacitance model or Meyer Capacitance model suffers from many shortcomings even for long-channel devices. In transient spice analysis, such a model does not conserve charge, Even by introducing errors in the simulations.



- a periodic rectangular waveform applied to a voltage divider consisting of an ideal capacitor and nonlinear capacitance drop at the output node because in every period some charge of node x is lost.
- This effect arises from the calculation of charge by integrating capacitor voltages with respect to time, an operation that accumulates small errors in the simulation.
- To minimize this type of error, the simulation algorithm can be modified without the user computer.
- The charge in the inversion layer, depletion layer and extrinsically partitions the charge among the three capacitances.
- partitioning a charge between source and drain terminals and bulk terminal.

5 (A) CMOS physical Structure:



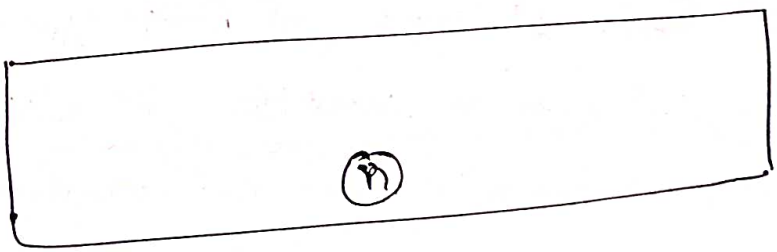


4M

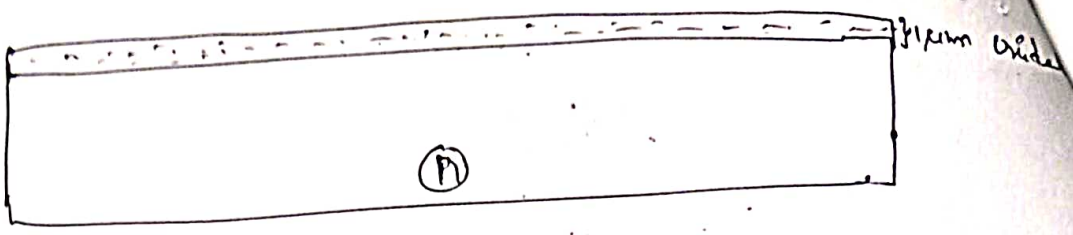
5 (B) CMOS is a Combination of pmos and NMOS. It can be fabricated in three ways.

(1) p-well process
(2) N-well process
(3) Twintub process

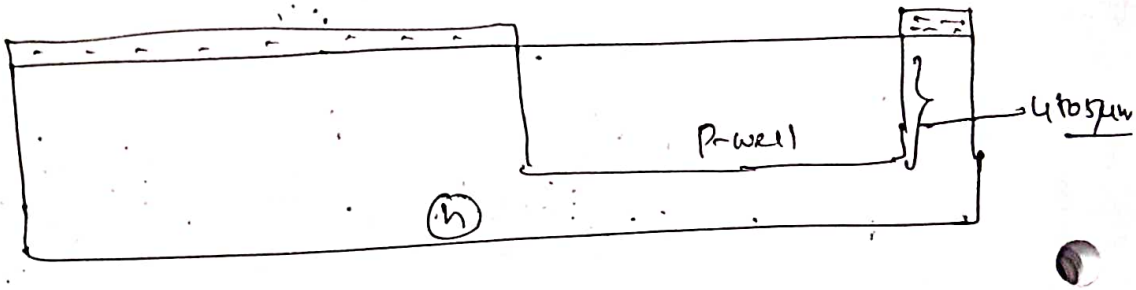
(1) p-well process: Take N-type substrate.



Step 2: formation of thick oxide layer

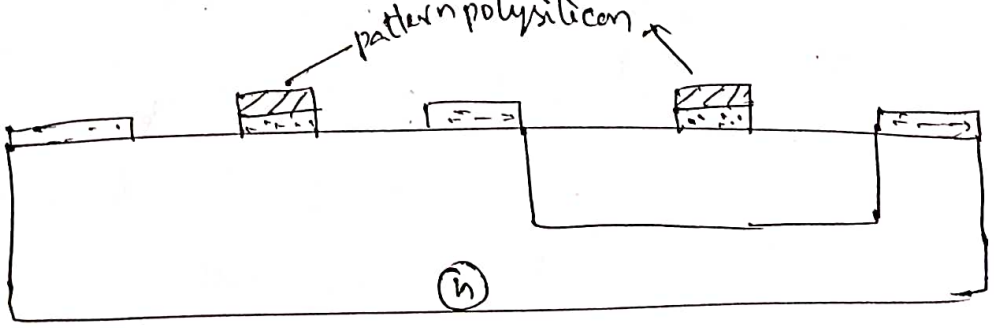


Step 3: Create p-well after etching the oxidation layer.



- n-type substrate is a parent substrate used for fabricating the pmos device.
- p-well is called child substrate, act as p-type substrate for fabricating the Nmos device. ——SM

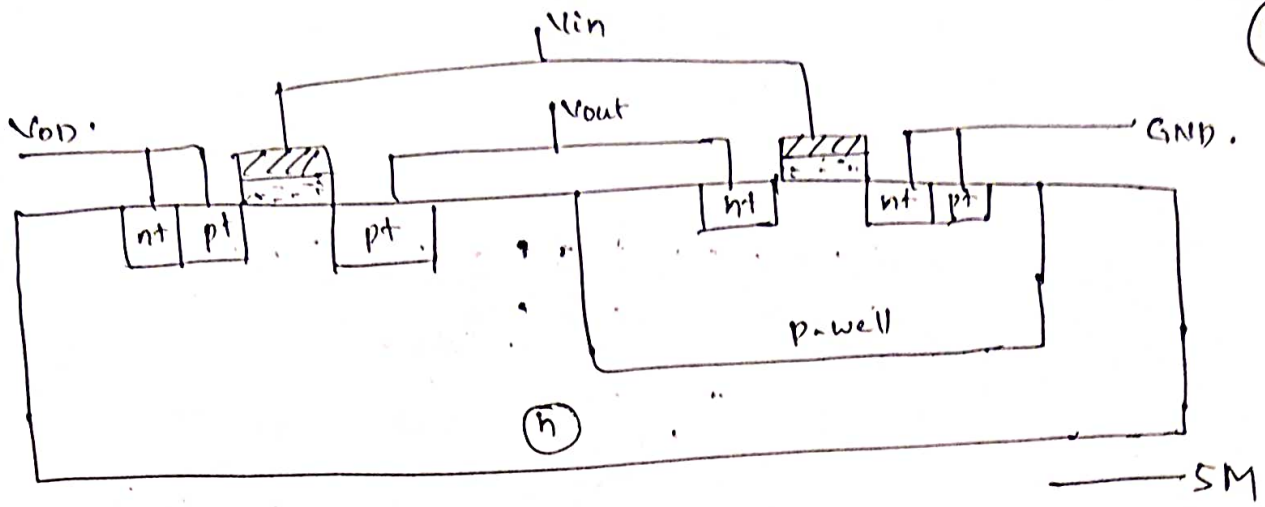
Step 4: deposet the pattern polysilicon for formation of gate terminals



Step 5: do the diffussion of n-type and p-type Impurities using p+ Mask and n+ mask.

p+ mask is used for p+ diffussion

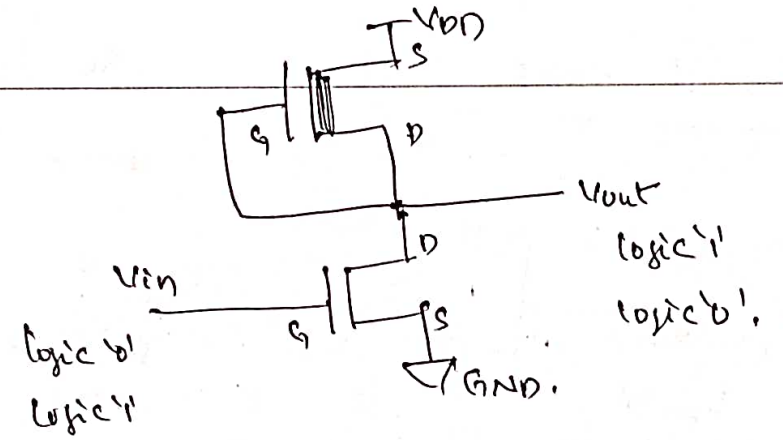
n+ mask is used for n-diffussion.

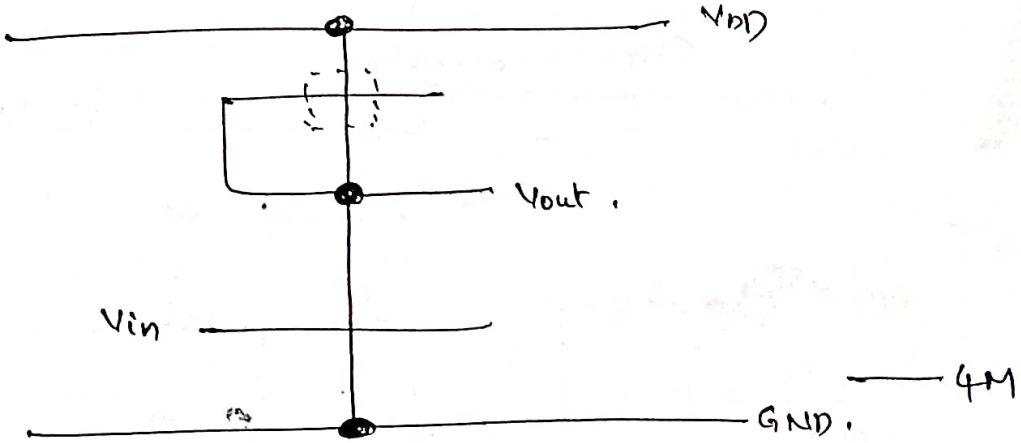


(6)(A) Stick diagram of NMOS Inverter :

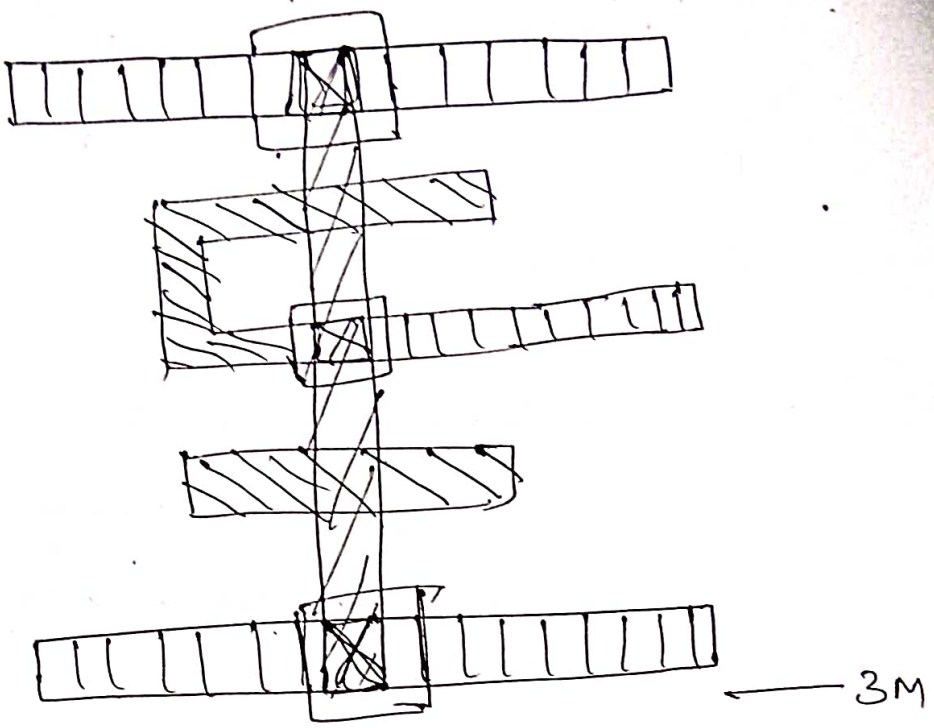
— Stick diagram is a planning of layout before designing a actual physical design which in placed on a substrate.

— Stick diagram does not follow any dimensions.

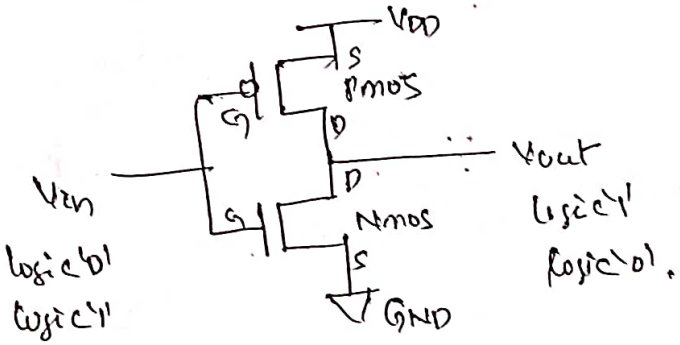




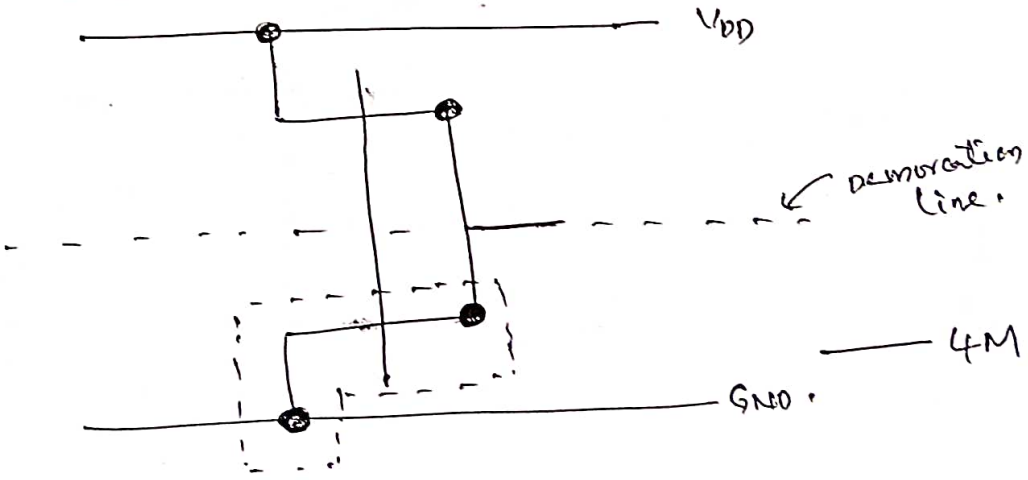
Layout of Nmos Inverter:



(6)(B). p-well CMOS Inverter:

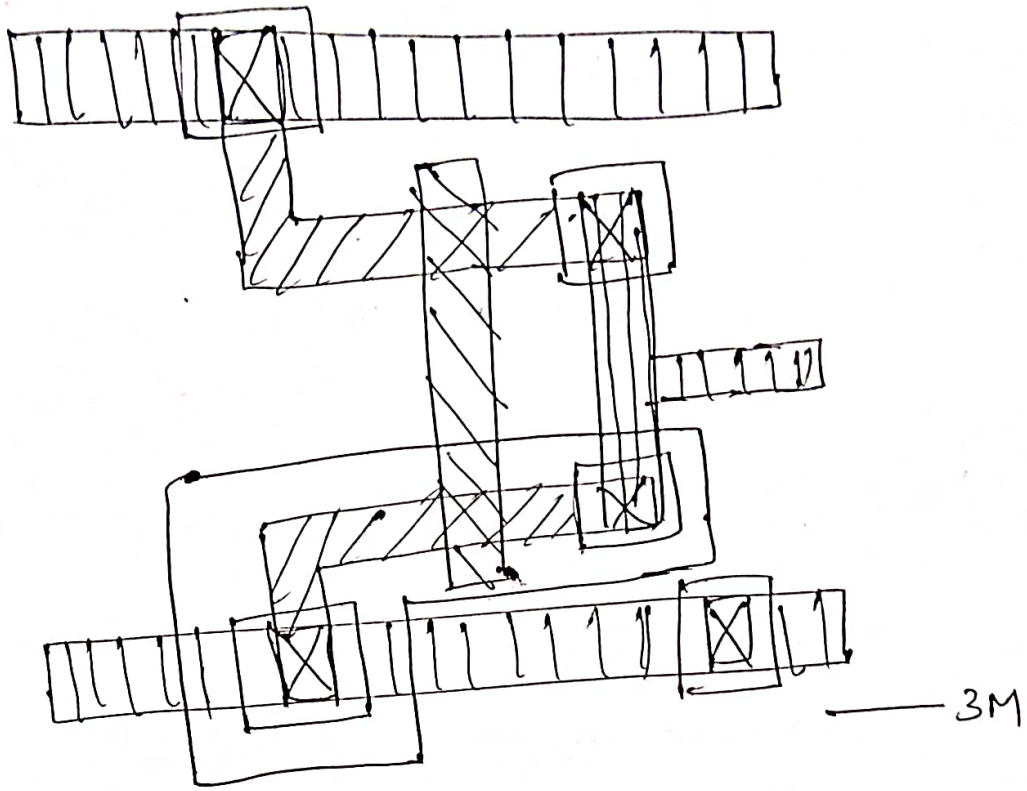


Stick diagram:



(R)

Layout :



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(7) (A)

Transconductance (g_m) :

Transconductance is the relation between the output current (I_{DS}) to input voltage (V_{gs}).

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{gs}}\right|_{V_{ds} = \text{Constant}}.$$

— Transconductance is should be high for any device.

Interms of circuit parameter,

$$I_{ds} = \frac{Q_c}{T} \qquad \left| \begin{array}{l} Q_c = C_g \cdot \partial V_{gs} \\ T = \frac{L^2}{\mu V_{ds}} \end{array} \right.$$

$$\boxed{g_m = \frac{C_g \mu \cdot V_{ds}}{L^2}}$$

In saturation region $V_{ds} = (V_{gs} - V_t)$

$$g_m = \frac{C_g \mu}{L^2} (V_{gs} - V_t) \qquad \because C_g = \frac{\varepsilon_{ins} \varepsilon_{oxi} WL}{D}$$

$$g_m = \frac{\mu \varepsilon_{ins} \varepsilon_0}{D} \frac{W}{L} (V_{gs} - V_t)$$

$$g_m = \beta \beta (V_{gs} - V_t) \qquad \text{—— SM}$$

(7) (B) **Output Conductance (g_{ds}):**

A reduction in channel length results in an increase in ω_0 owing to the higher g_m. However, the gain of the MOS device decrease owing to the strong degradation of the output resistance.

$$\text{Output resistance} = \frac{1}{g_{ds}}$$

Output Conductance can be expressed

$$g_{ds} = \frac{\partial I_{DS}}{\partial V_{ds}} = \lambda \cdot I_{ds} \propto \left(\frac{1}{L}\right)^2$$

Here strong dependence on the channel length is demonstrated as

$$\lambda \propto \frac{1}{L} \quad \text{and} \quad I_{ds} \propto \frac{1}{L}.$$

→ Small g_{ds} increase the voltage gain, which is benficial for analog and digital circuit Applications. —— SM

(4) (c). - Switching an enhancement mode mos transistor from the OFF to ON state consists in applying sufficient gate voltage to neutralize the charges and enables the underlying silicon to undergo an inversion due to the electric field from the gate.

- Switching a depletion mode nmos transistor from the ON to OFF state consists in applying enough voltage to the gate to add to the stored charge and invert the 'n' implant region to 'p'.

The threshold voltage V_t may be expressed as

$$V_t = \phi_{ms} - \frac{Q_B - Q_{ss}}{C_o} + 2\phi_{fN}$$

Q_B = charge per unit area

Q_{ss} = charge density at $Si:SiO_2$ interface.

C_o = Capacitance per unit gate area

ϕ_{ms} = work function difference between gate and Si

ϕ_{fN} = Fermi level potential between inverted surface and bulk Si. ——— 4M.

Prepared by

26/11/21

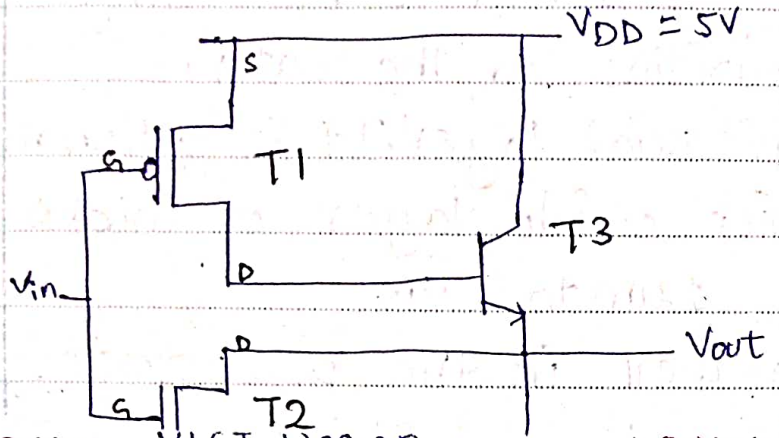
(Dr. C. Venkataiah)

Dept. of ECE.

26.12.2021

(ESTD-1995)

1a) Bi-CMOS inverter with no static current flow:-



Subject: VLSI Design

Q.P. Code: A0426197R1222

For Office Use
13426043

VALUATION-II							
Q.No.	1	2	3	4	5	6	7
A							
B							
C							
D							
E							
F							
G							
TOTAL							
GRAND TOTAL							

(in words)

Signature of the Examiner

Signature of the Scrutinizer

Subject: VLSI Design

Q.P. Code: A0426197R1222

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VALUATION-I							
Q.No.	1	2	3	4	5	6	7
A	✓	6	7		4	4	4
B	2	7	6		9	~~8~~	4
C	✓						3
D	✓						
E	✓						
F	✓						
G	✓						
TOTAL	14	13	13		13	4	11
GRAND TOTAL	64						

(in words) Six Four

Signature of the Examiner

Signature of the Scrutinizer

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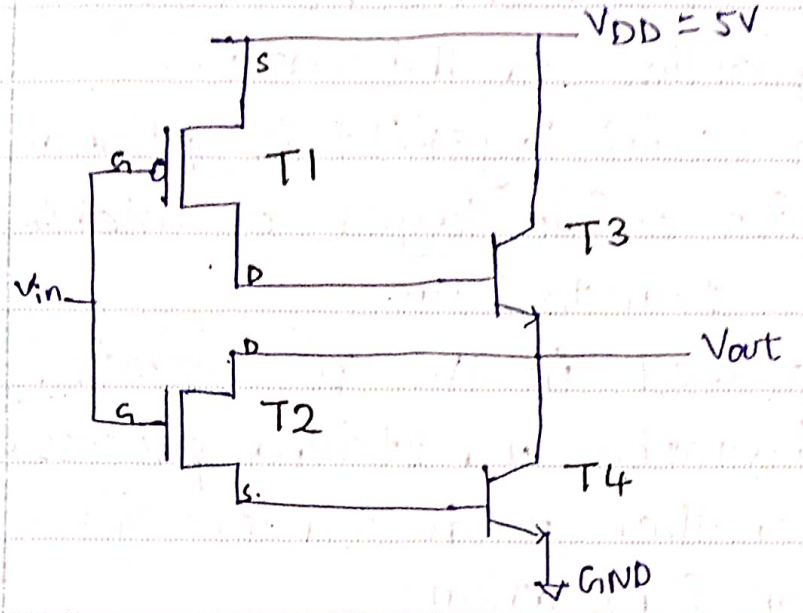
(ESTD 1905)

1a) Bi-CMOS inverter with no static current flow:-



=>When input Vin = logic '0'
Transistors T1 and T3 are in 'ON' state
Output Vout = logic '1'

=> When input Vin = logic '1'
Transistors T2 and T4 are 'ON' and T1, T3 are OF
Output is Vout = logic '0'

=> By connecting the NMOS drain to output static current flow is reduced.

Advantages:-

1. Static current flow is reduced.
2. High speed due to CMOS circuit
3. Output driving capability is high due to BJT.

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Q.No	Marks
1a	2

Q.No	Marks

Q.No	Marks

(ESTD-1995)

1b) Steps in n-well process:-

1. Preparation of p-substrate by doping the p-type impurities to the wafer.
2. Formation of Epitaxial layer. It is optional.
3. Formation of thick oxide layer of thickness ranging from 1 um to 2 um
4. Formation of n-well in the p-substrate using photolithography and Etching process.
5. Formation of another oxide window for n-mos transistor fabrication
6. Formation of thin oxide layer (1 um)
7. Depositing pattern polysilicon on the top of oxide layers of both windows to form gate terminal using glass mask.
8. Diffusion of p^+-impurities in the n-well to form p-mos and n^+-impurities in p-substrate to form n-mos using glass mask.
9. Formation of metallic layer for the purpose of interconnecting of terminals in the CMOS.
10. Connecting the terminals to powersupply and ground for the operation.

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10	7

Q.No	Marks
01	

(ESTD-1995)

1c) Fringing fields:

The fields which are produced in the circuit between the different components due to the parameters of current, voltage are called fringing fields.

=> The fields which causes the fringing field capacitance are called fringing fields.

=> Fringing field capacitance of a circuit is given by

$$C_{ff} = \varepsilon_{SiO_2} \varepsilon_0 L \left\{ \frac{\pi}{1 + \frac{2d}{t}\left(1 + \frac{t}{d}\right)} - \frac{t}{2d} \right\}$$

1d) Threshold voltage:

=> The minimum voltage required to form the channel between source and drain terminals of MOSFET is called threshold voltage.

=> In other words, the minimum voltage required to activate the device or to 'ON' the device is called threshold voltage.

=> When the input is greater than threshold voltage then channel is formed.

=> In general, threshold voltage of MOSFET is given as $V_{th} = 0.2\, V_{DD}$

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Q.No	Marks
1c	2

Q.No	Marks
1d	2

Q.No	Marks

(ESTD-1995)

1e) Transistor sizing:-

=> Transistor sizing is nothing but reducing the size of transistor to acheive low power design.

=> Transistor sizing is done by scaling the parameters of transistor like length of channel, width of channel, thickness of oxide layer, depth of diffusion.

=> To reduce the parameters we use scaling factors α and β. α is for length, width and depth of diffusion. β is for thickness of oxide.

1f) CMOS λ-based design rules

=> CMOS λ-based design rules are the dimensions of the layout to be fabricated

=> λ-based rules converts the stick diagram into layout design.

=> It is used for better design of layout

=> All dimensions are in λ. So the name is λ-based design rules.

=> For example, the width of active area is 3λ

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Q.No	Marks

Q.No	Marks
1e	✓

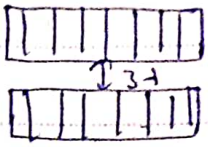
Q.No	Marks
1f	

(ESTD-1995)

=> 2. Width of Contact is 2λ x 2λ

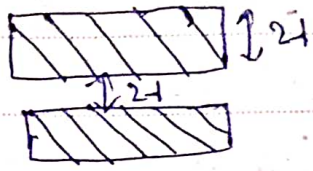
3. Metal width is 3λ

4. Metal spacing is 3λ



5. Polysilicon width is 2λ

6. polysilicon spacing is 2λ

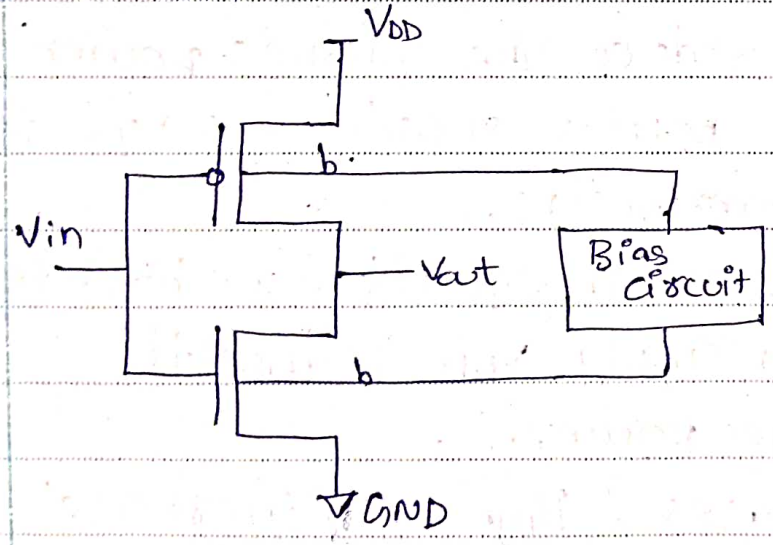


1g) Body effect:-

=> Body effect is defined as applying the bias voltage to the body terminal of the MOSFET to reduce the threshold voltage.

=> It is also known as Body biasing.

=> It is acheived by using Substrate bias circuit.



=> It reduces the Vo threshold voltage So dynamic power decreases or reduced.

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Q.No	Marks
1f	✓

Q.No	Marks
1g	✓

Q.No	Marks

2a) Voltage Scaling:-

=> Voltage Scaling is defined as the reducti of supply voltage of a circuit.

=> That is, reducing the value of power supply

=> Voltage scaling is used to reduce the dynamic power dissipation which is occurs during switching activity.

=> We have the dynamic power as

$$P_{dyn} = \alpha_T C_L f_{clk} V_{DD}^2$$

here, α_T is node transition factor

C_L is load capacitance of circuit

f_{clk} is operating frequency of circuit

V_{DD}^2 is supply power

=> It is easy to reduce the dynamic power by reducing the power supply voltage to that of other parameters.

=> From the dynamic power equation we have to know that power supply V_{DD} is directly proportional to the power.

=> If V_{DD} increases, P_{dyn} also increases and V_{DD} is decreases, P_{dyn} also decreases.

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Q.No	Marks

Q.No	Marks
2a	

Q.No	Marks
7a	

(ESTD-1995)

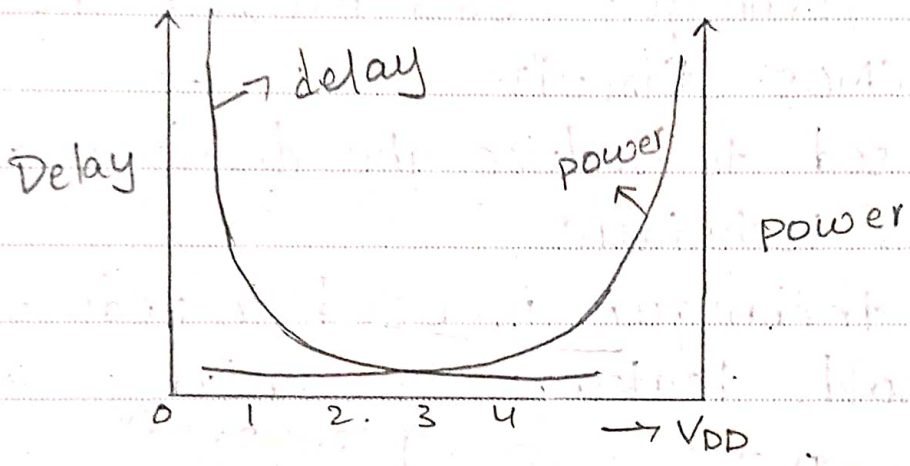
=> But the problem here to reduce the power supply voltage is risetime or fall time of a circuit.

=> We have a relation between rise or fall time to V_{DD} as

$$t_r = \frac{3 C_L}{B_P V_{DD}}$$

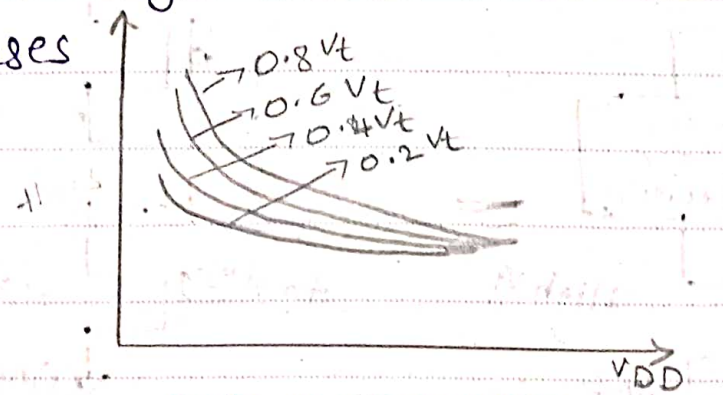
=> V_{DD} is inversly proportional to the delay.

=> If V_{DD} is reduced, delay increases.



If V_{DD} decreases, threshold voltage also decreases.

If threshold voltage decreases sub-threshold leakage current increases



For the use of Evaluator Only

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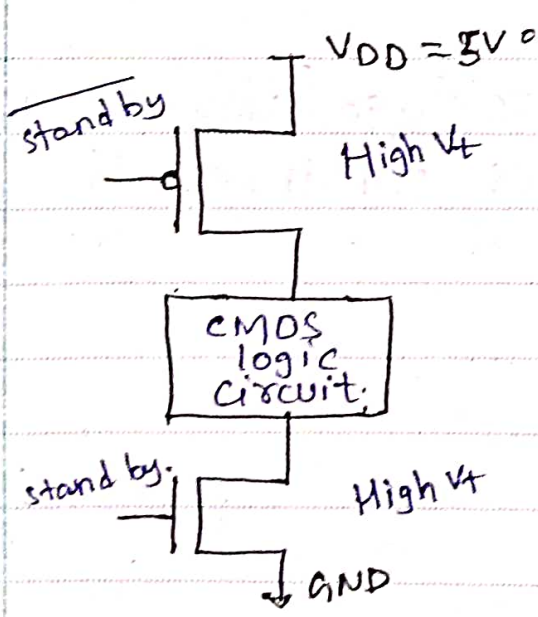
If the sub-threshold voltage leakage current increases the device damages.
To reduce sub-threshold vo leakage current.
There are two techniques:-
1. VTCMOS [Variable threshold voltage CMOS]
2. MTCMOS [Multiple threshold voltage CMOS]

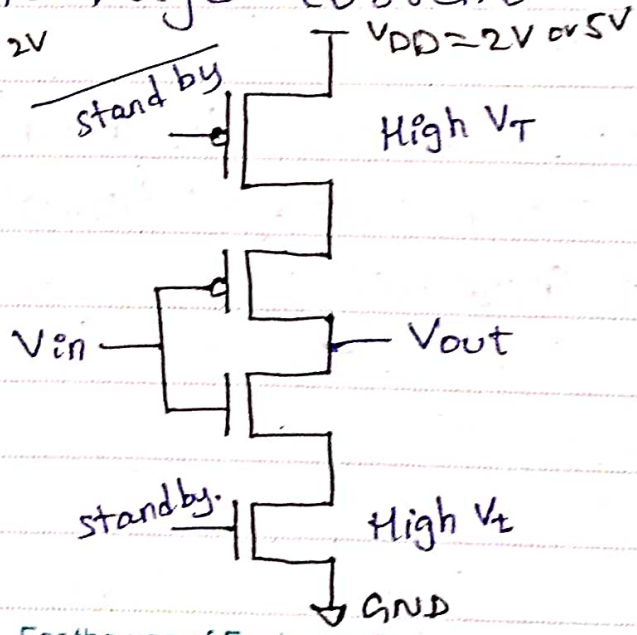
2b) MTCMOS technique:-

=> MTCMOS technique uses Multiple threshold voltage CMOS circuit.

=> It is used to reduce the disadvantages of VTCMOS technique

=> MTCMOS technique is used to reduce the sub-threshold leakage current.





For the use of Evaluator Only

Q.No	Marks

Q.No	Marks
2a	6

Q.No	Marks

(ESTD-1995)

=> MTCMOS consists of two type transistors which have different threshold voltages.

=> The actual CMOS inverter circuit has low threshold voltage.

=> This low threshold voltage circuit is conneted with two High threshold voltage transistors.

=> If the circuit is 'ON' power supply is connected to 2V and threshold voltage is 0.2V.

=> If the circuit is 'OFF' power supply is connected to 5V and threshold voltage is 0.8V

Advantages:

1. Sub-threshold leakage current is reduced by providing different voltages of threshold and by using different V_T transistors. and powersupplis
2. Dynamic power also reduces by reducing voltage
3. Speed increases
4. Fabrication of MTCMOS also easy because there is no extra circuit

Disadvantage:-

1. No. of transistors increases due to the addition of High Vt transistors.

For the use of Evaluator Only

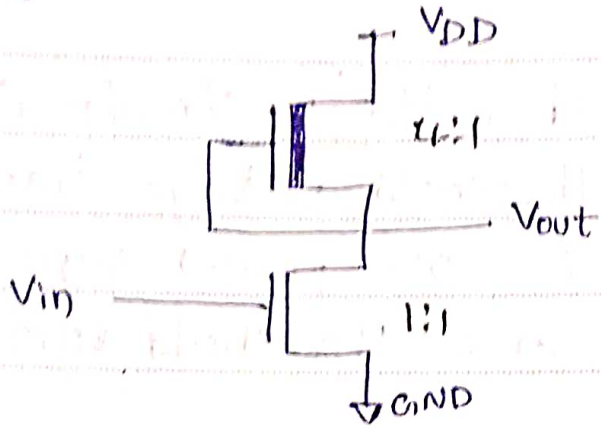
Q.No	Marks

Q.No	Marks
26	7

Q.No	Marks

3 a) Resistance for NMOS inverter:

The circuit diagram of NMOS inverter is given as



For NMOS inverter z is as 4:1

i.e $z = z_{pu} : z_{pd}$.

$z_{pu} = 4:1$ and $z_{pd} = 1:1$

For the resistance calculation we have

$R = Z R_s$.

R_s is the sheet resistance of the device

For pull-up transistor.

$R_{pu} = z_{pu} R_s$

for NMOS at 5 μm technology $R_s = 10^4 \Omega$

$R_{pu} = \frac{4}{1} \times 10^4$

$R_{pu} = 4 \times 10^4 \Omega$

$R_{pu} = 40 K\Omega$

For the use of Evaluator Only

Q.No	Marks

Q.No	Marks

Q.No	Marks

(ESTD-1995)

For pull-down transistor

$R_{Pd} = Z_{Pd} R_s$

for NMOS at 5μm technology $R_s = 10^4 \Omega$

$R_{Pd} = \frac{1}{1} \times 10^4 \Omega$

$R_{Pd} = 10^4 \Omega$

$\boxed{R_{Pd} = 10 k\Omega}$

Total resistance for NMOS inverter is the sum of the resistances offered by pull-up and pull-down transistor. Because for any input both the transistors are active

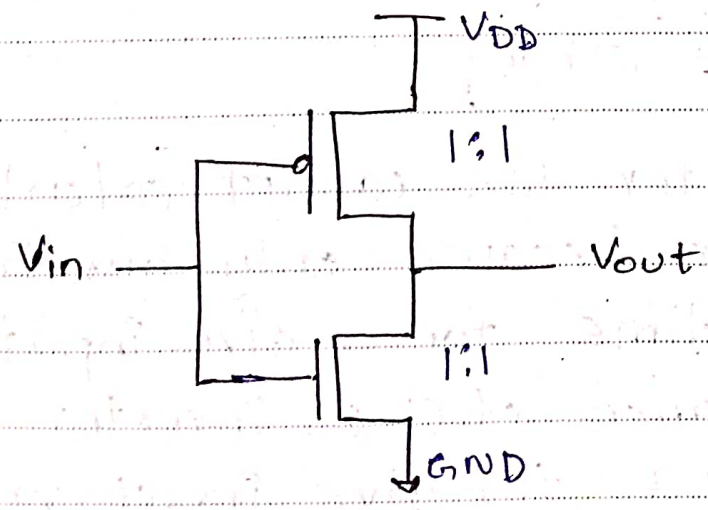
$\therefore \quad R = R_{PU} + R_{Pd}$

$R = 40 k\Omega + 10 k\Omega$

$\boxed{R = 50 k\Omega}$

Resistance for CMOS inverter:

The CMOS circuit diagram is as follows



For the use of Evaluator Only

Q.No	Marks

Q.No	Marks

Q.No	Marks

(ESTD-1995)

For CMOS inverter Z is 1:1

$Z = \frac{L}{W}$ ratio

$Z = Z_{PU} : Z_{Pd}$

$Z_{PU} = 1:1$ and $Z_{Pd} = 1:1$

For pull-up transistor.

$R_{PU} = Z_{PU} R_S$

Pull-up transistor is PMOS and for PMOS at 5um technology $R_S = 2.5 \times 10^4 \Omega$

$R_{PU} = \frac{1}{1} \times 2.5 \times 10^4 \Omega$

$\boxed{R_{PU} = 25\ k\Omega}$

For pull-down transistor:

$R_{Pd} = Z_{Pd} \cdot R_S$

For NMOS at 5um technology $R_S = 10^4 \Omega$

$R_{Pd} = \frac{1}{1} \times 10^4 \Omega$

$\boxed{R_{Pd} = 10\ k\Omega}$

For CMOS inverter we cannot calculate the total resistance because only one transistor is 'ON' at a time for a give input logic. So the resistance of CMOS inverter is either 25 kΩ or 10kΩ for give input value

For the use of Evaluator Only

Q.No	Marks

Q.No	Marks
30	✗

Q.No	Marks

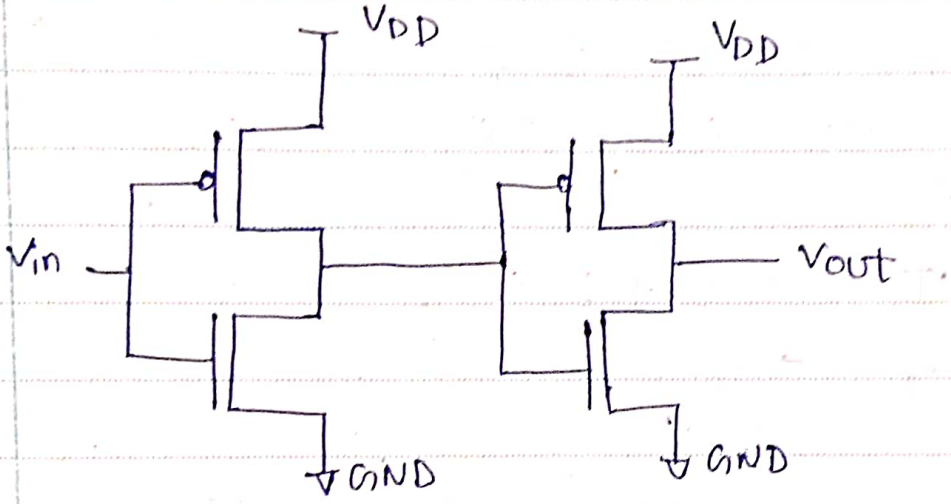
(ESTD 1995)

3b) Delay of two stage CMOS inverter.

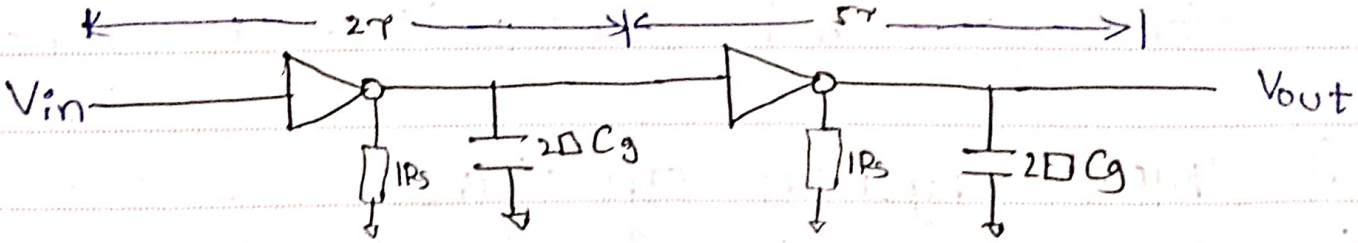
=> Delay time is defined as one square standard capacitance charged through one square n-channel nmos transistor resistance

=> It is given as $\tau = 1R_s \times 1\square C_g$.

=> Two stage CMOS inverter is as follows.



It is also represent as follow in simple.



For the first CMOS inverter circuit

$\tau = 10^4 \times 2\square C_g$

$\tau = 20k = 2\tau$

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Q.No	Marks

Q.No	Marks

Q.No	Marks

For second stage CMOS inverter

$T = R_s \times 2\square C_g$

$T = 2.5 \times 10^4 \times 2\square C_g$

$T = 50K = 5\tau$

As CMOS has PMOS and NMOS only one is active at a time, consider Vin is logic 1 So the delay for first stage is 2τ and for second stage is 5τ

Total delay of two stage CMOS inverter is

$$T = 2\tau + 5\tau$$

$$\boxed{T = 7\tau}$$

In general, $\tau = 0.3$ nsec is a better delay for 5um technology and 0.2 nsec for 2um technology and 0.1 nsec for 1.2um technology

5a) CMOS physical structure.

=> CMOS is a complimentary mosfet.

=> It contains both CMOS and NMOS

=> It gives complimentary output for a given input.

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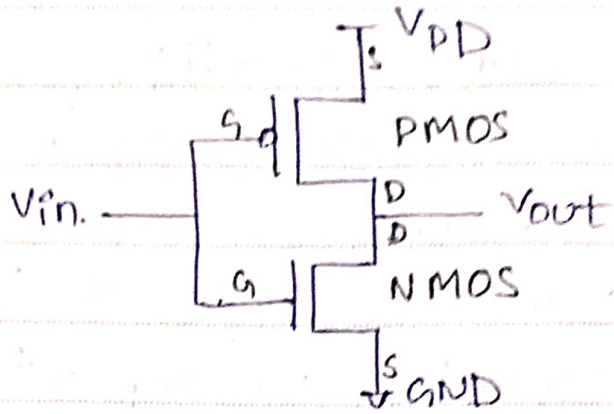
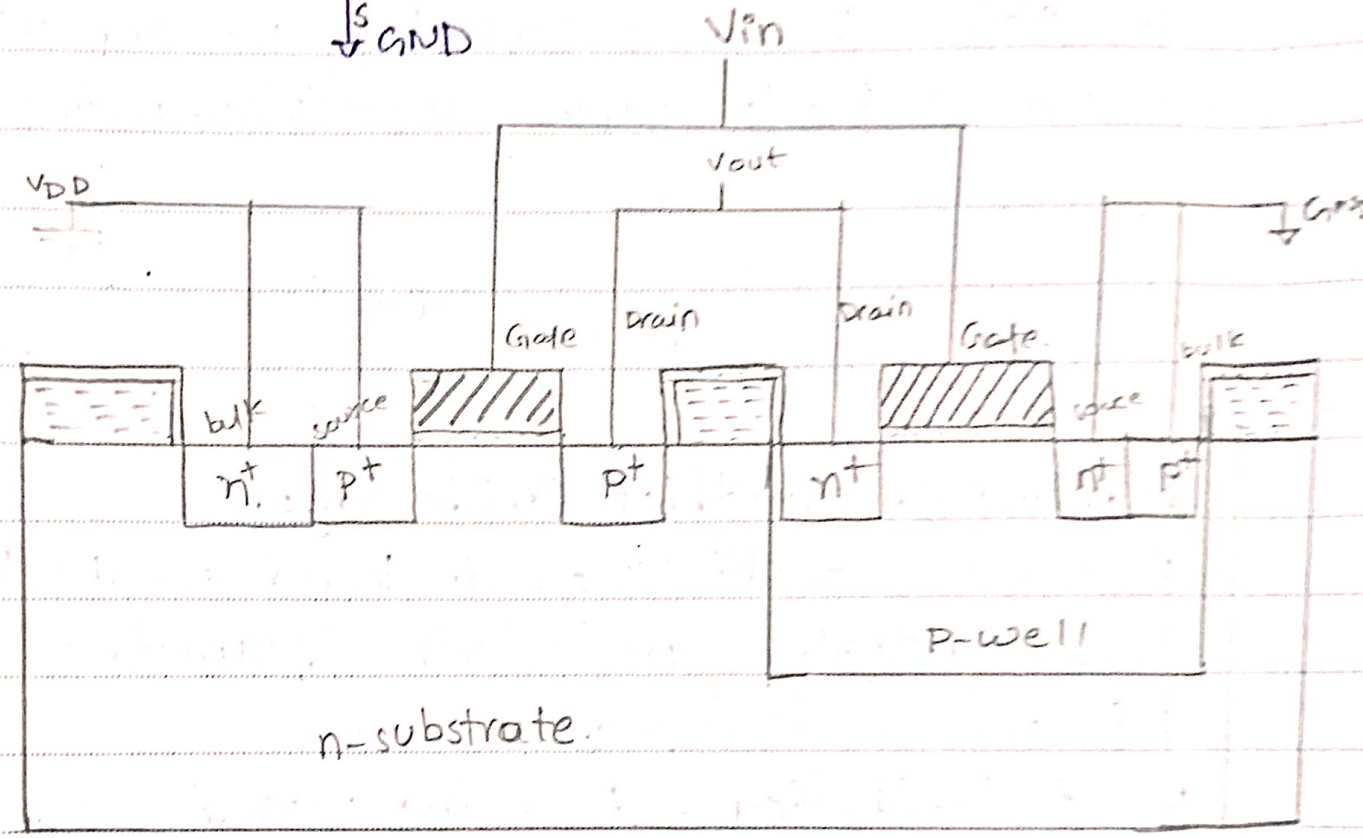
Q.No	Marks

Q.No	Marks
3b	6

Q.No	Marks





Above is the physical structure of the CMOS using p-well process.

Other techniques also there to fabricate the cmos inverter. They are:-

1. p-well process
2. n-well process
3. Twin-tub process.

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Q.No	Marks

Q.No	Marks
5a	4

Q.No	Marks

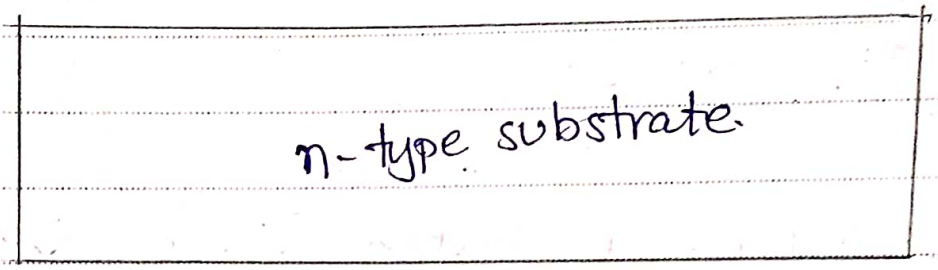
(ESTD-1995)

5b) CMOS fabrication using P-well:-

=> For P-well n-type substrate is used.

1. Formation of n-type substrate:

n-type substrate is formed by doping the n-type impurities to the wafer by ion implantation method or chemical vapour deposition method.



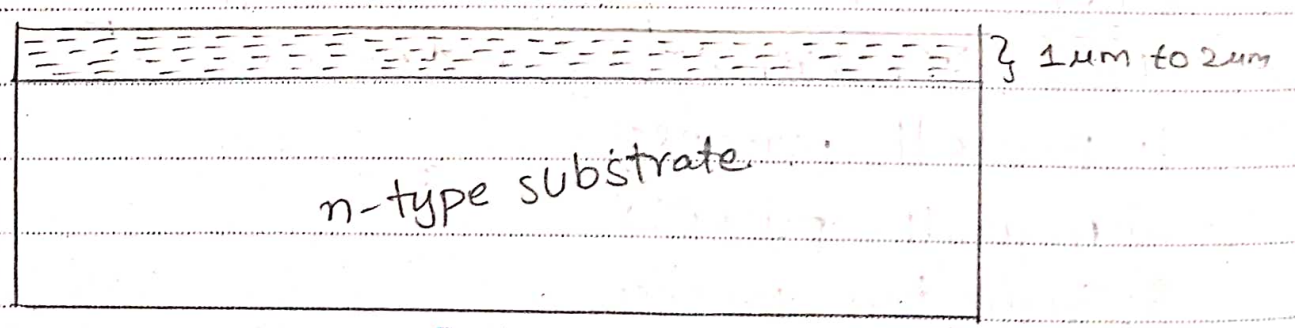
2. Formation of thick Oxide layer:

Formation of thick oxide layer on the top of the substrate of width 1um to 2um

It can be done in two ways.

1. Wet oxidation :- By using water
2. Dry oxidation :- By using pure oxygen.

$$Si + 2H_2O \longrightarrow SiO_2 \text{ (wet)}$$
$$Si + O_2 \longrightarrow SiO_2 \text{ (dry)}$$



For the use of Evaluator Only

Q.No	Marks

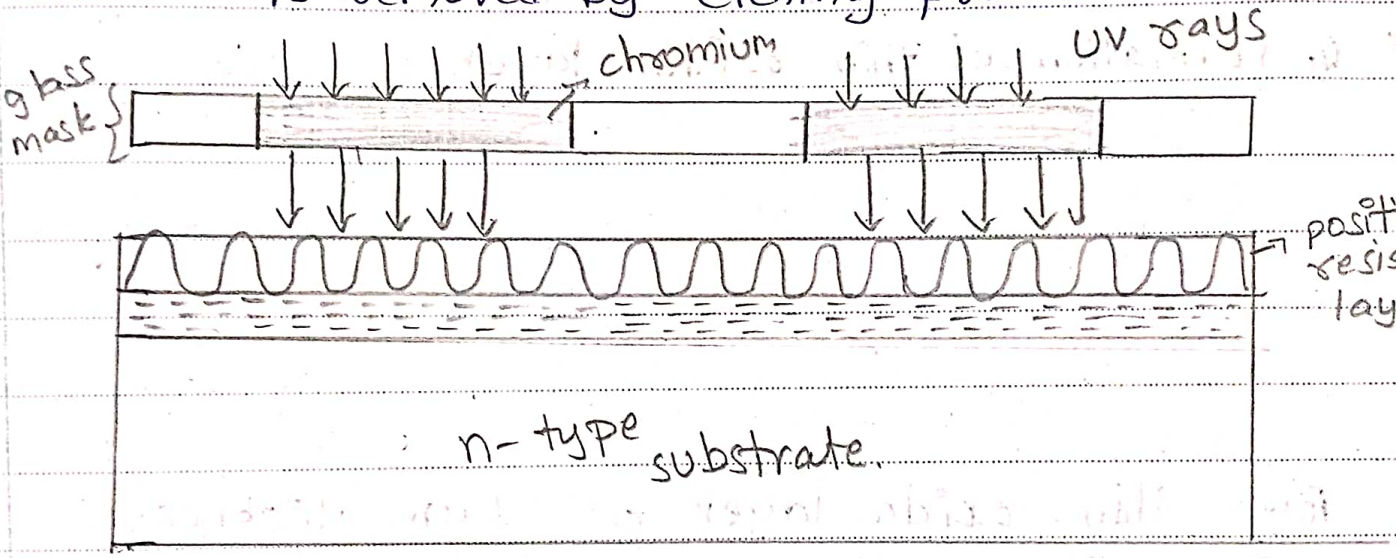
Q.No	Marks

Q.No	Marks

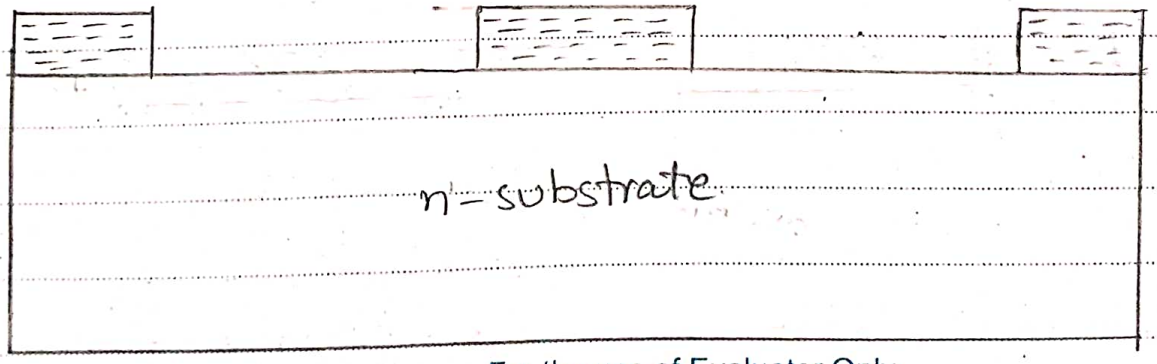
(ESTD 1995)

3. Formation of p-well oxide window:

To form the p-well we have to do photolithogr-aphy and etching process to remove the oxide layer. Another window also formed by same process Photoresistive layer are formed on substrate and it is subjected to UV rays through a glass mask with chromium which allows the UV rays through it The part which is subjected to UV rays becomes soft and it is removed by etching process.



Etching process



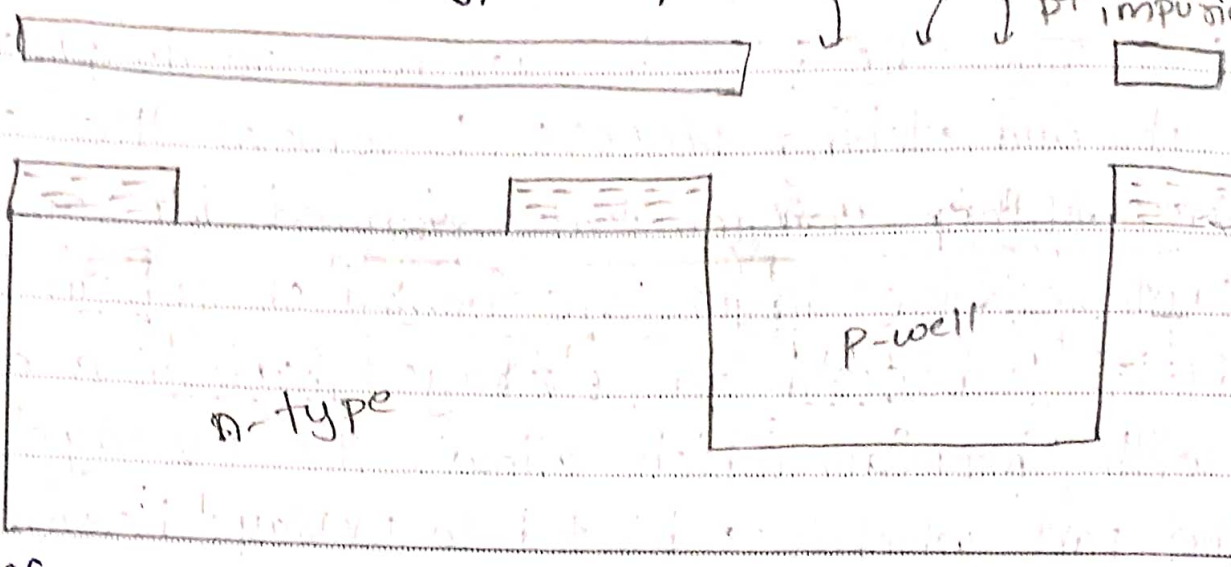
For the use of Evaluator Only

Q.No	Marks

Q.No	Marks

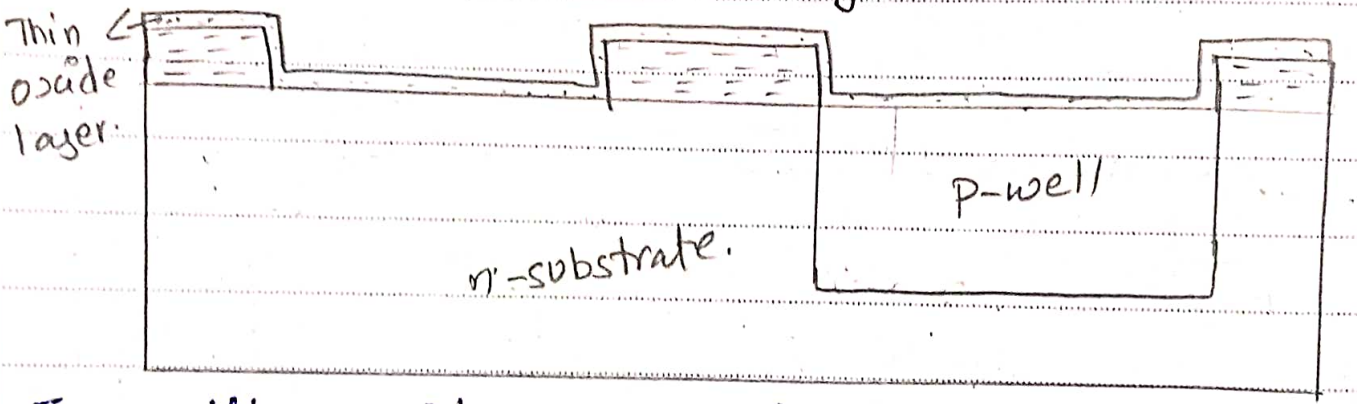
Q.No	Marks

4. 4) Diffuse the P-type impurities to form P-well.



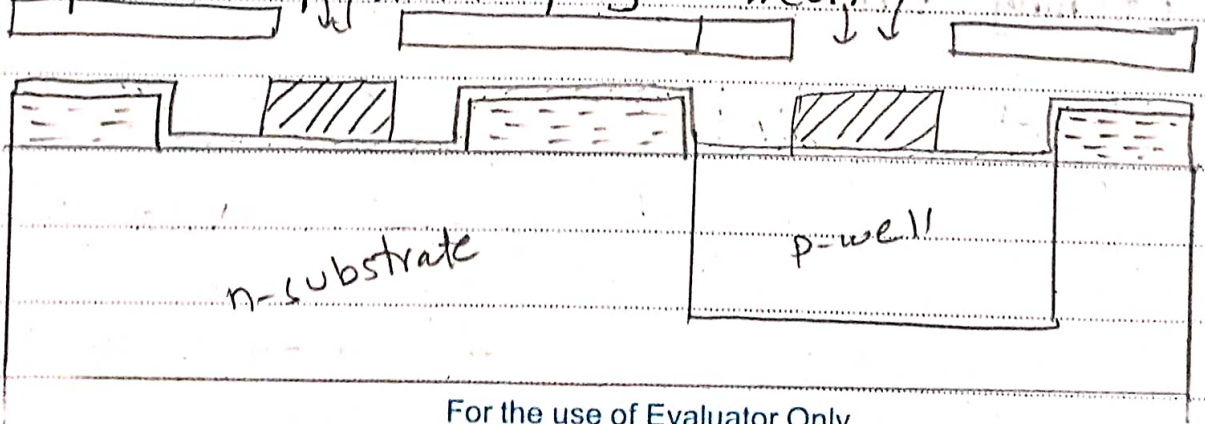
Diffuse P type impurities using glass mask.

5. 5) Formation of thin oxide layer.



Form thin oxide layer of 1μm thickness.

6. Deposite pattern poly silicon



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Q.No	Marks

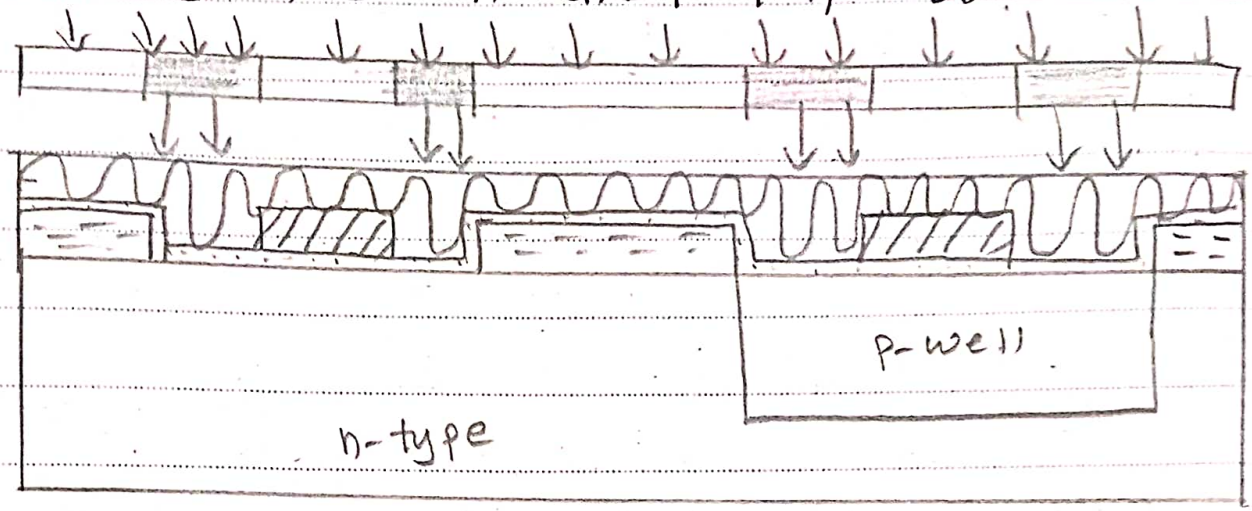
Q.No	Marks

Q.No	Marks

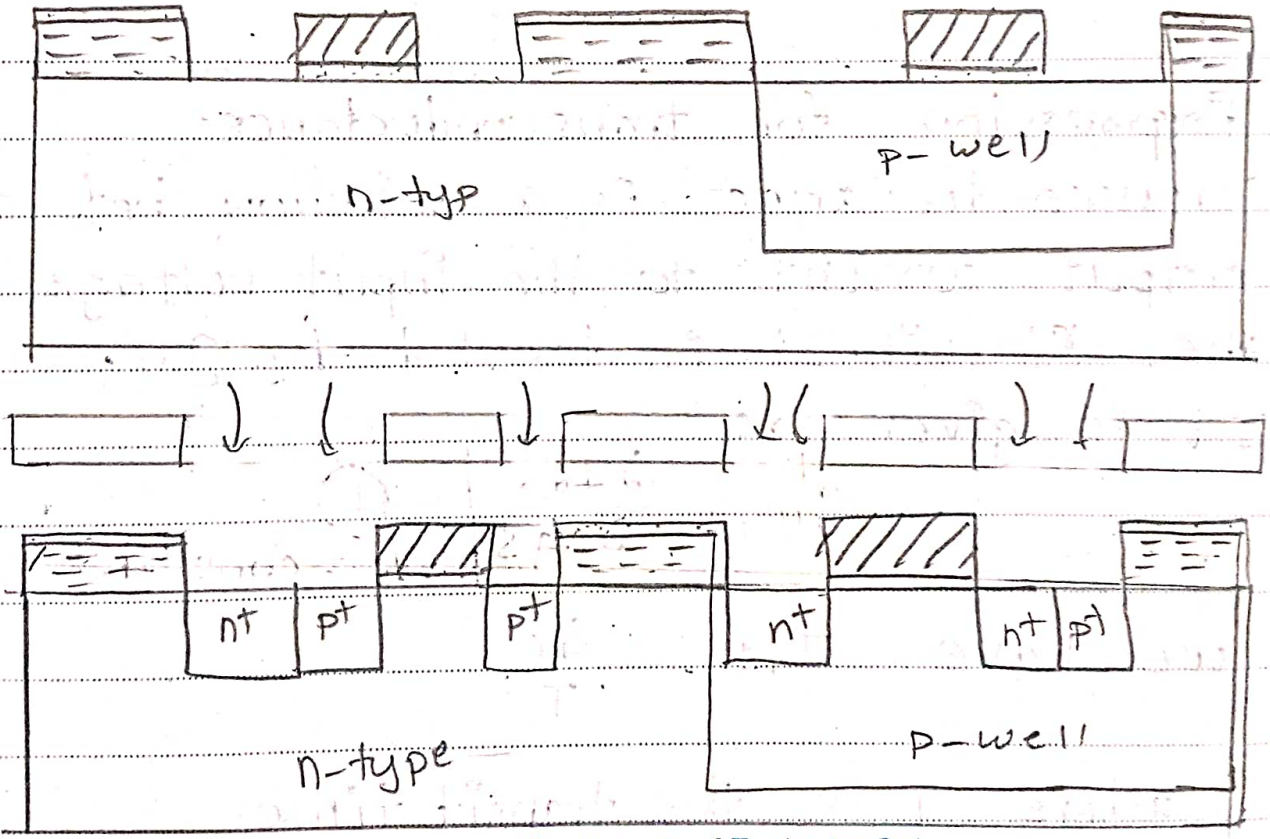
(ESTD-1995)

Deposite the pattern poly silicon by using glass mask to form gate terminal on both windows

7. Diffuse the n^+ and p^+ impurities.



Etching process



For the use of Evaluator Only

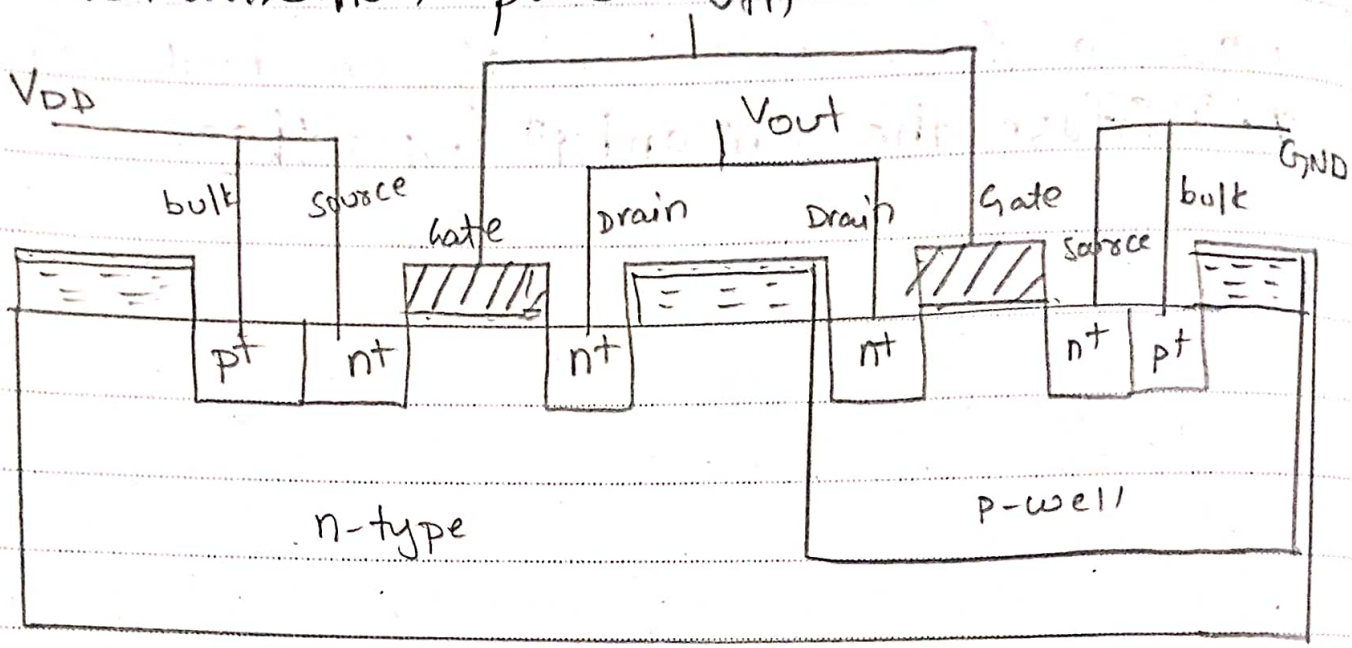
Q.No	Marks

Q.No	Marks

Q.No	Marks

(ESTD-1995)

8. Metallization process



metallization is used to interconnect the terminals of CMOS.

7a) Expression for transconductance:

Transconductance is a relation between output current to the input voltage of the circuit. It is denoted by g_m.

It is given as

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}=\text{constant}} \quad \leftarrow (1)$$

we have $I_{ds} = \frac{Q_c}{T}$

where T is the transit time

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Q.No	Marks

Q.No	Marks
5b	9

Q.No	Marks

Q_c is the charge of the electron.

T is given as

$$T = \frac{L^2}{\mu V_{ds}}$$

and $Q = CV$

$$Q_c = C_g V_{gs}$$

Therefore

$$I_{ds} = \frac{C_g V_{gs}}{\frac{L^2}{\mu V_{ds}}}$$

$$I_{ds} = \frac{C_g V_{gs} \mu V_{ds}}{L^2}$$

$$\partial I_{ds} = \frac{C_g V_{ds} \mu \partial V_{gs}}{L^2} \quad \text{—(2)}$$

sub (2) in (1)

$$g_m = \frac{C_g V_{ds} \mu \partial V_{gs}}{L^2 \cdot \partial V_{gs}}$$

$$\boxed{g_m = \frac{C_g V_{ds} \mu}{L^2}}$$

$$C_g = C_o W L$$

$$g_m = \frac{C_o W L V_{ds} \mu}{L^2}$$

For the use of Evaluator Only

Q.No	Marks

Q.No	Marks

Q.No	Marks

(ESTD-1995)

$$g_m = \frac{C_o \, w \, \mu \, V_{ds}}{L}$$

For saturation $V_{ds} = V_{gs} - V_t$

$$g_m = C_o \mu \left(\frac{w}{L}\right)(V_{gs} - V_t)$$

7b) Output conductance g_{ds}:-

Output conductance (g_{ds}) is defined as the relation between output current to output voltage. It is denoted by g_{ds}. It is given as

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} \Big|_{V_{gs} = \text{constant}}$$

$$g_{ds} = \frac{1}{R_{ds}}$$

where R_{ds} = output resistance.

$$I_{ds} = \frac{Q_c}{T}$$

$$= \frac{C_g \cdot V_{gs}}{\frac{L^2}{\mu V_{ds}}}$$

$$= \frac{C_g V_{gs} \mu V_{ds}}{L^2}$$

For the use of Evaluator Only

Q.No	Marks

Q.No	Marks
7c	4

Q.No	Marks

(ESTD-1995)

$$\partial I_{ds} = \frac{C_g V_{gs} \mu}{L^2} \partial V_{ds}$$

Therefore, $g_{ds} = \frac{C_g V_{gs} \mu \partial V_{ds}}{L^2 \partial V_{ds}}$

$$g_{ds} = \frac{C_g V_{gs} \mu}{L^2}$$

$$g_{ds} = \frac{C_g \omega L \mu V_{gs}}{L^2}$$

$$\boxed{g_{ds} = \frac{C_o \omega \mu V_{gs}}{L}}$$

For saturation $V_{ds} = V_{gs} - V_t$

$$V_{gs} = V_{ds} + V_t$$

$$g_{ds} = \frac{C_o \omega \mu (V_{ds} + V_t)}{L}$$

7C) Threshold voltage (V_t):-

Threshold voltage is defined as the minimum voltage required to form the channel between source and drain of a MOSFET.

It is denoted by V_t.

In general threshold voltage of a transisto is given as $\boxed{V_t = 0.2\ V_{DD}}$

here, V_{DD} is power supply voltage of circuit

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Q.No	Marks
7b	4

Q.No	Marks

Q.No	Marks

From the transconductance of saturation region

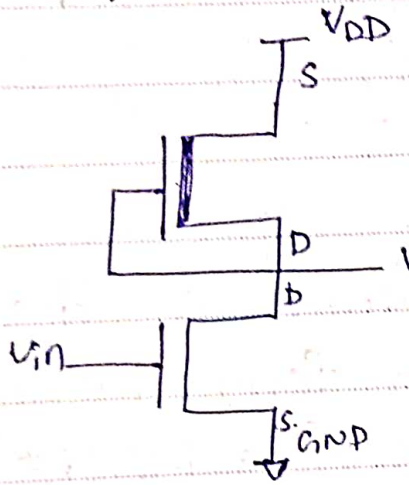
$$g_m = \frac{C_o W_M}{L}(V_{gs} - V_t)$$

$$\frac{g_m L}{C_o W_M} = V_{gs} - V_t$$

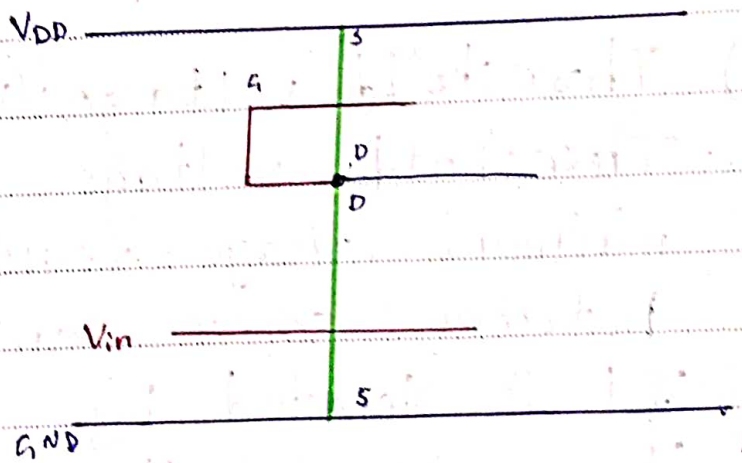
$$\frac{g_m L}{C_o W_M} - V_{gs} = -V_t$$

$$\boxed{V_t = V_{gs} - \frac{g_m L}{C_o W_M}}$$

6a) NMOS inverter.



stick diagram



For the use of Evaluator Only

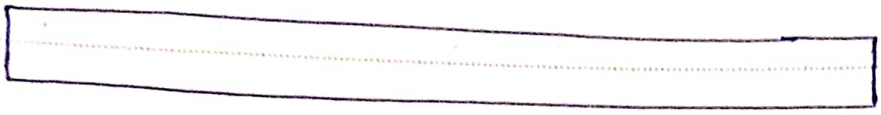
Q.No	Marks

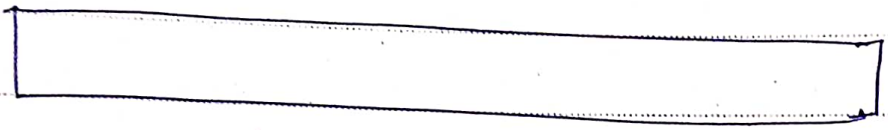
Q.No	Marks
XC	3

Q.No	Marks

(ESTD-1995)

Layout





For the use of Evaluator Only

Q.No	Marks

Q.No	Marks
6a	4

Q.No	Marks

(ESTD-1995)

For the use of Evaluator Only

Q.No	Marks

Q.No	Marks

Q.No	Marks

CO- PO Attainment

Academic Year :2022-23

Regulations :R19

Year :IV,Sem-1

Batch :19

Branch :ECE

Subject(Code) :VLSI Design

Name of the Faculty :Dr. C. Venkataiah

External Question Paper Marks --> Cos							
Q.No.	CO 1	CO 2	CO 3	CO 4	CO 5	CO 6	Total
1 a)	2						2
b)	2						2
c)			2				2
d)				2			2
e)					2		2
f)		2					2
g)					2		2
2 a)				7			7
b)				7			7
c)							0
3 a)			7				7
b)			7				7
c)							0
4 a)					7		7
b)					7		7
c)							0
5 a)	4						4
b)	10						10
c)							0
6 a)		7					7
b)		7					7
c)							0
7 a)	5						5
b)	5						5
c)	4						4
Total	32	16	16	16	18	0	98

Mid I Marks --> Cos							
Q.No.	CO 1	CO 2	CO 3	CO 4	CO 5	CO 6	Total
1 a)	1						1
b)			1				1
c)		1					1
d)	1						1
e)			1				1
2 a)	3						3
b)				2			2
3 a)			3				3
b)					2		2
4 a)					3		3
b)		2					2
5 a)			3				3
b)			2				2
Total	5	3	10	2	5	0	25

Mid II Marks --> Cos							
Q.No.	CO 1	CO 2	CO 3	CO 4	CO 5	CO 6	Total
1 a)	1						1
b)		1					1
c)			1				1
d)				1			1
e)					1		1
2 a)	2						2
b)				3			3
3 a)		3					3
b)					2		2
4 a)			3				3
b)				2			2
5 a)					3		3
b)	2						2
Total	5	4	4	6	6	0	25

Total	10	7	14	8	11	0	50

Assignment 1 Marks --> Cos							
	CO 1	CO2	CO3	CO4	CO5	CO6	Total
	2	2	2	2	2		10
Total	2	2	2	2	2	0	10

Assignment 2 Marks --> Cos							
	CO1	CO2	CO3	CO4	CO5	CO6	Total
	2	2	2	2	2		10
Total	2	2	2	2	2	0	10

Total	4	4	4	4	4	0	20
Total	4	4	4	4	4	0	20

	CO 1		CO 2		CO 3		CO 4		CO 5		CO 6	
	No. of students Attained	Weightage Points	No. of students Attained	Weightage Points	No. of students Attained	Weightage Points	No. of students Attained	Weightage Points	No. of students Attained	Weightage Points	No. of students Attained	Weightage Points
>= 65%	195	3	214	3	221	3	215	3	216	3	0	3
40% to 65%	69	2	51	2	45	2	50	2	49	2	0	2
<40%	3	1	2	1	1	1	2	1	2	1	0	1
Total No. of stud	267		267		267		267		267		0	
Atainment value		2.72		2.79		2.82		2.80		2.80		0.00
% of Attainment		73.03		80.15		82.77		80.52		80.90		0.00
Attained or not		YES		YES		YES		YES		YES		0.00

IV Year Threshold
65

CO	CO Attainment Value	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	2.72	3	2											2		
CO 2	2.79		2	3											1	
CO 3	2.82	1	1	3												2
CO 4	2.80						3	2						2		
CO 5	2.80											2	3			2
CO 6	0.00	0	0	0	0	0	0	0	0	0	0	0	0			
VLSI Design		2.75	2.77	2.81	-	-	2.80	2.80	-	-	-	2.80	2.80	2.76	2.79	2.81

S.No	Reg.No.	"Internal marks"	"Assignment marks"	"Final Internal marks"	"Total Final Marks"	"External Marks"
1	19091A0405	19	10	29	79	50
2	19091A0407	18	10	28	79	51
3	19091A0408	19	10	29	85	56
4	19091A0411	19	10	29	87	58
5	19091A0413	19	10	29	86	57
6	19091A0414	16	10	26	83	57
7	19091A0415	18	10	28	86	58
8	19091A0416	19	10	29	79	50
9	19091A0421	19	10	29	89	60
10	19091A0423	17	10	27	90	63
11	19091A0429	19	10	29	79	50
12	19091A0434	18	10	28	83	55
13	19091A0436	18	10	28	89	61
14	19091A0441	18	10	28	78	50
15	19091A0442	14	10	24	80	56
16	19091A0444	19	10	29	78	49
17	19091A0450	19	10	29	89	60

18	19091A0451	19	10	29	88	59
19	19091A0452	19	10	29	87	58
20	19091A0459	19	10	29	90	61
21	19091A0463	17	10	27	75	48
22	19091A0466	19	10	29	89	60
23	19091A0474	18	10	28	86	58
24	19091A0478	19	10	29	93	64
25	19091A0482	19	10	29	67	38
26	19091A0486	19	10	29	91	62
27	19091A0488	16	10	26	60	34
28	19091A0489	19	10	29	91	62
29	19091A04A0	19	10	29	92	63
30	19091A04A1	19	10	29	92	63
31	19091A04A5	19	10	29	94	65
32	19091A04B3	19	10	29	95	66
33	19091A04B5	19	10	29	89	60
34	19091A04C6	19	10	29	95	66
35	19091A04C9	19	10	29	66	37
36	19091A04D6	19	10	29	93	64
37	19091A04D9	16	10	26	72	46
38	19091A04E1	18	10	28	83	55
39	19091A04E3	17	10	27	73	46
40	19091A04E4	19	10	29	91	62
41	19091A04E5	17	10	27	83	56
42	19091A04E8	19	10	29	93	64
43	19091A04F9	19	10	29	89	60
44	19091A04G1	19	10	29	88	59
45	19091A04G2	19	10	29	89	60
46	19091A04G7	19	10	29	82	53
47	19091A04G8	19	10	29	76	47
48	19091A04H3	19	10	29	76	47

49	19091A04J4	19	10	29	87	58
50	19091A04K0	19	10	29	86	57
51	19091A04K5	17	10	27	86	59
52	19091A04K7	18	10	28	85	57
53	19091A04K8	18	10	28	92	64
54	19091A04M2	19	10	29	76	47
55	19091A04M3	18	10	28	87	59
56	19091A04M5	19	10	29	90	61
57	19091A04M9	19	10	29	88	59
58	19091A04N2	19	10	29	91	62
59	19091A04N6	19	10	29	71	42
60	19091A04P0	19	10	29	93	64
61	19091A04P4	19	10	29	95	66
62	19091A04Q1	19	10	29	87	58
63	19091A04Q6	15	10	25	75	50
64	19091A04R1	18	10	28	88	60
65	19091A04S0	18	10	28	88	60
66	19091A04S2	19	10	29	95	66
67	19091A04S5	18	10	28	81	53
68	19091A04S6	19	10	29	89	60
69	20095A0401	19	10	29	81	52
70	20095A0423	19	10	29	65	36
71	18091A04A3	17	10	27	73	46
72	19091A0404	17	10	27	80	53
73	19091A0410	17	10	27	80	53
74	19091A0417	18	10	28	73	45
75	19091A0419	14	10	24	73	49
76	19091A0424	19	10	29	91	62
77	19091A0426	17	10	27	81	54
78	19091A0428	17	10	27	72	45
79	19091A0431	12	10	22	65	43

80	19091A0432	19	10	29	79	50
81	19091A0437	18	10	28	80	52
82	19091A0446	14	10	24	49	25
83	19091A0454	17	10	27	71	44
84	19091A0455	16	10	26	58	32
85	19091A0456	15	10	25	60	35
86	19091A0460	17	10	27	77	50
87	19091A0462	18	10	28	85	57
88	19091A0464	16	10	26	69	43
89	19091A0467	17	10	27	73	46
90	19091A0469	18	10	28	81	53
91	19091A0479	18	10	28	85	57
92	19091A0480	19	10	29	91	62
93	19091A0481	18	10	28	87	59
94	19091A0490	16	10	26	84	58
95	19091A0491	13	10	23	64	41
96	19091A0495	15	10	25	80	55
97	19091A0498	18	10	28	89	61
98	19091A04A4	13	10	23	82	59
99	19091A04A6	18	10	28	91	63
100	19091A04A7	17	10	27	87	60
101	19091A04A9	18	10	28	93	65
102	19091A04B1	15	10	25	88	63
103	19091A04B4	19	10	29	96	67
104	19091A04B9	17	10	27	83	56
105	19091A04C2	15	10	25	88	63
106	19091A04C4	18	10	28	91	63
107	19091A04C5	19	10	29	90	61
108	19091A04C8	19	10	29	87	58
109	19091A04D2	16	10	26	80	54
110	19091A04D8	14	10	24	70	46

111	19091A04E0	17	10	27	70	43
112	19091A04E7	18	10	28	78	50
113	19091A04E9	19	10	29	86	57
114	19091A04F0	18	10	28	78	50
115	19091A04F6	19	10	29	83	54
116	19091A04F8	13	10	23	64	41
117	19091A04G0	13	10	23	74	51
118	19091A04G9	16	10	26	64	38
119	19091A04H2	17	10	27	62	35
120	19091A04H4	12	10	22	63	41
121	19091A04J2	14	10	24	77	53
122	19091A04K2	14	10	24	78	54
123	19091A04K6	18	10	28	80	52
124	19091A04M1	13	10	23	57	34
125	19091A04M8	17	10	27	80	53
126	19091A04N3	18	10	28	84	56
127	19091A04N5	16	10	26	75	49
128	19091A04N7	15	10	25	80	55
129	19091A04P1	17	10	27	85	58
130	19091A04P8	19	10	29	84	55
131	19091A04Q2	19	10	29	68	39
132	19091A04Q3	16	10	26	79	53
133	19091A04R2	18	10	28	80	52
134	19091A04R4	16	10	26	70	44
135	19091A04S1	17	10	27	79	52
136	20095A0403	19	10	29	89	60
137	20095A0410	17	10	27	75	48
138	20095A0413	14	10	24	58	34
139	20095A0415	18	10	28	68	40
140	20095A0422	16	10	26	68	42
141	18091A0485	15	10	25	63	38

142	19091A0418	16	10	26	78	52
143	19091A0422	17	10	27	78	51
144	19091A0430	12	10	22	64	42
145	19091A0438	13	10	23	53	30
146	19091A0440	16	10	26	71	45
147	19091A0443	12	10	22	68	46
148	19091A0448	16	10	26	61	35
149	19091A0457	18	10	28	65	37
150	19091A0468	15	10	25	73	48
151	19091A0470	16	10	26	75	49
152	19091A0472	17	10	27	80	53
153	19091A0473	9	10	19	69	50
154	19091A0476	13	10	23	65	42
155	19091A0477	16	10	26	72	46
156	19091A0483	14	10	24	74	50
157	19091A0487	14	10	24	65	41
158	19091A0494	17	10	27	87	60
159	19091A0497	11	10	21	68	47
160	19091A0499	18	10	28	86	58
161	19091A04A2	16	10	26	87	61
162	19091A04A8	15	10	25	55	30
163	19091A04B0	17	10	27	65	38
164	19091A04B2	14	10	24	59	35
165	19091A04B8	18	10	28	89	61
166	19091A04C0	13	10	23	76	53
167	19091A04D0	14	10	24	80	56
168	19091A04D1	13	10	23	48	25
169	19091A04D7	13	10	23	67	44
170	19091A04E2	15	10	25	77	52
171	19091A04E6	13	10	23	61	38
172	19091A04F3	16	10	26	73	47

173	19091A04F5	15	10	25	71	46
174	19091A04G3	17	10	27	83	56
175	19091A04G4	13	10	23	70	47
176	19091A04H5	12	10	22	78	56
177	19091A04H7	12	10	22	63	41
178	19091A04H8	15	10	25	73	48
179	19091A04J5	19	10	29	84	55
180	19091A04J6	15	10	25	76	51
181	19091A04J7	15	10	25	50	25
182	19091A04J8	18	10	28	79	51
183	19091A04K1	19	10	29	76	47
184	19091A04K4	13	10	23	54	31
185	19091A04M0	13	10	23	65	42
186	19091A04M4	16	10	26	66	40
187	19091A04N1	13	10	23	64	41
188	19091A04P2	12	10	22	64	42
189	19091A04P3	14	10	24	71	47
190	19091A04P7	17	10	27	75	48
191	19091A04Q0	14	10	24	65	41
192	19091A04Q4	15	10	25	76	51
193	19091A04Q5	17	10	27	76	49
194	19091A04R0	16	10	26	55	29
195	19091A04R5	15	10	25	73	48
196	19091A04R6	15	10	25	73	48
197	19091A04R7	15	10	25	56	31
198	19091A04S3	15	10	25	79	54
199	19091A04S4	12	10	22	58	36
200	20095A0405	17	10	27	70	43
201	20095A0406	17	10	27	74	47
202	20095A0408	18	10	28	71	43
203	20095A0409	15	10	25	59	34

204	20095A0412	16	10	26	70	44
205	20095A0416	17	10	27	67	40
206	20095A0417	18	10	28	64	36
207	20095A0419	18	10	28	66	38
208	20095A0425	19	10	29	79	50
209	19091A0401	11	10	21	68	47
210	19091A0402	11	10	21	62	41
211	19091A0403	13	10	23	48	25
212	19091A0420	11	10	21	66	45
213	19091A0425	13	10	23	59	36
214	19091A0427	15	10	25	60	35
215	19091A0435	18	10	28	68	40
216	19091A0439	17	10	27	70	43
217	19091A0445	11	10	21	40	19
218	19091A0447	12	10	22	38	16
219	19091A0449	18	10	28	67	39
220	19091A0453	12	10	22	67	45
221	19091A0458	19	10	29	78	49
222	19091A0461	12	10	22	51	29
223	19091A0465	15	10	25	61	36
224	19091A0475	16	10	26	75	49
225	19091A0484	16	10	26	69	43
226	19091A0492	15	10	25	80	55
227	19091A0493	14	10	24	75	51
228	19091A0496	13	10	23	69	46
229	19091A04A3	14	10	24	69	45
230	19091A04B7	16	10	26	80	54
231	19091A04C7	14	10	24	73	49
232	19091A04D3	19	10	29	67	38
233	19091A04D4	16	10	26	80	54
234	19091A04D5	17	10	27	83	56

235	19091A04F4	13	10	23	50	27
236	19091A04F7	18	10	28	77	49
237	19091A04G5	18	10	28	73	45
238	19091A04G6	14	10	24	57	33
239	19091A04H0	15	10	25	60	35
240	19091A04H1	14	10	24	56	32
241	19091A04H6	16	10	26	75	49
242	19091A04H9	14	10	24	68	44
243	19091A04J0	10	10	20	30	10
244	19091A04J1	14	10	24	71	47
245	19091A04J3	13	10	23	72	49
246	19091A04J9	14	10	24	68	44
247	19091A04K3	16	10	26	64	38
248	19091A04K9	18	10	28	65	37
249	19091A04M6	12	10	22	63	41
250	19091A04M7	16	10	26	74	48
251	19091A04N0	13	10	23	59	36
252	19091A04N8	15	10	25	73	48
253	19091A04P5	10	10	20	53	33
254	19091A04P6	12	10	22	53	31
255	19091A04P9	10	10	20	46	26
256	19091A04Q7	16	10	26	76	50
257	19091A04Q8	15	10	25	74	49
258	19091A04R3	17	10	27	82	55
259	19091A04R9	9	10	19	53	34
260	20095A0402	13	10	23	70	47
261	20095A0404	18	10	28	86	58
262	20095A0407	16	10	26	63	37
263	20095A0411	18	10	28	74	46
264	20095A0414	15	10	25	65	40
265	20095A0418	14	10	24	51	27

266	20095A0420	8	10	18	43	25
267	20095A0424	19	10	29	79	50

% of IM	% of AM	% of EM	N CO 1	N CO 2	N CO 3	N CO 4	N CO 5
95	100	71.42857	76.6761	79.0166	81.36851	79.40108	79.7816872
90	100	72.85714	77.11457	79.15996	80.75504	79.42072	79.5930479
95	100	80	83.46535	85.05282	86.51652	85.2921	85.504451
95	100	82.85714	85.72843	87.06489	88.23252	87.25577	87.412039
95	100	81.42857	84.59689	86.05885	87.37452	86.27393	86.458245
80	100	81.42857	82.51768	83.47082	82.9601	83.38733	83.0309453
90	100	82.85714	85.03536	86.20221	86.76105	86.29357	86.2696058
95	100	71.42857	76.6761	79.0166	81.36851	79.40108	79.7816872
95	100	85.71429	87.99151	89.07696	89.94852	89.21944	89.319627
85	100	90	90	90.36972	89.57958	90.24055	89.8961424
95	100	71.42857	76.6761	79.0166	81.36851	79.40108	79.7816872
90	100	78.57143	81.64074	83.1841	84.18704	83.34806	83.4082238
90	100	87.14286	88.42999	89.22032	89.33505	89.23908	89.1309877
90	100	71.42857	75.98303	78.15392	79.89704	78.43888	78.6392539
70	100	80	80	80.73944	79.15916	80.4811	79.7922849
95	100	70	75.54455	78.01056	80.51051	78.41924	78.8278932
95	100	85.71429	87.99151	89.07696	89.94852	89.21944	89.319627
95	100	84.28571	86.85997	88.07093	89.09052	88.2376	88.365833
95	100	82.85714	85.72843	87.06489	88.23252	87.25577	87.412039
95	100	87.14286	89.12306	90.083	90.80652	90.20128	90.2734209
85	100	68.57143	73.02687	75.27918	76.70957	75.51301	75.5892327
95	100	85.71429	87.99151	89.07696	89.94852	89.21944	89.319627
90	100	82.85714	85.03536	86.20221	86.76105	86.29357	86.2696058
95	100	91.42857	92.51768	93.10111	93.38052	93.14678	93.1348029
95	100	54.28571	63.0976	66.94416	71.0725	67.61905	68.3361594
95	100	88.57143	90.2546	91.08903	91.66452	91.18311	91.2272149
80	100	48.57143	56.49222	60.33199	63.22608	60.80511	61.0936838
95	100	88.57143	90.2546	91.08903	91.66452	91.18311	91.2272149
95	100	90	91.38614	92.09507	92.52252	92.16495	92.1810089
95	100	90	91.38614	92.09507	92.52252	92.16495	92.1810089
95	100	92.85714	93.64922	94.10714	94.23852	94.12862	94.0885969
95	100	94.28571	94.78076	95.11318	95.09653	95.11046	95.0423908
95	100	85.71429	87.99151	89.07696	89.94852	89.21944	89.319627
95	100	94.28571	94.78076	95.11318	95.09653	95.11046	95.0423908
95	100	52.85714	61.96605	65.93813	70.2145	66.63721	67.3823654
95	100	91.42857	92.51768	93.10111	93.38052	93.14678	93.1348029
80	100	65.71429	70.07072	72.40443	73.52209	72.58714	72.5392115
90	100	78.57143	81.64074	83.1841	84.18704	83.34806	83.4082238
85	100	65.71429	70.76379	73.2671	74.99356	73.54934	73.6816448

95	100	88.57143		90.2546	91.08903	91.66452	91.18311	91.2272149
85	100	80		82.07921	83.32746	83.57357	83.3677	83.2195846
95	100	91.42857		92.51768	93.10111	93.38052	93.14678	93.1348029
95	100	85.71429		87.99151	89.07696	89.94852	89.21944	89.319627
95	100	84.28571		86.85997	88.07093	89.09052	88.2376	88.365833
95	100	85.71429		87.99151	89.07696	89.94852	89.21944	89.319627
95	100	75.71429		80.07072	82.03471	83.94251	82.34659	82.6430691
95	100	67.14286		73.28147	75.99849	78.79451	76.45557	76.9203052
95	100	67.14286		73.28147	75.99849	78.79451	76.45557	76.9203052
95	100	82.85714		85.72843	87.06489	88.23252	87.25577	87.412039
95	100	81.42857		84.59689	86.05885	87.37452	86.27393	86.458245
85	100	84.28571		85.47383	86.34557	86.14758	86.31321	86.0809665
90	100	81.42857		83.90382	85.19618	85.90305	85.31173	85.3158118
90	100	91.42857		91.82461	92.23843	91.90905	92.18459	91.9923696
95	100	67.14286		73.28147	75.99849	78.79451	76.45557	76.9203052
90	100	84.28571		86.1669	87.20825	87.61905	87.27541	87.2233997
95	100	87.14286		89.12306	90.083	90.80652	90.20128	90.2734209
95	100	84.28571		86.85997	88.07093	89.09052	88.2376	88.365833
95	100	88.57143		90.2546	91.08903	91.66452	91.18311	91.2272149
95	100	60		67.62376	70.96831	74.5045	71.54639	72.1513353
95	100	91.42857		92.51768	93.10111	93.38052	93.14678	93.1348029
95	100	94.28571		94.78076	95.11318	95.09653	95.11046	95.0423908
95	100	82.85714		85.72843	87.06489	88.23252	87.25577	87.412039
75	100	71.42857		73.90382	75.5659	75.48263	75.55228	75.2119542
90	100	85.71429		87.29844	88.21429	88.47705	88.25724	88.1771937
90	100	85.71429		87.29844	88.21429	88.47705	88.25724	88.1771937
95	100	94.28571		94.78076	95.11318	95.09653	95.11046	95.0423908
90	100	75.71429		79.37765	81.17203	82.47104	81.38439	81.5006359
95	100	85.71429		87.99151	89.07696	89.94852	89.21944	89.319627
95	100	74.28571		78.93918	81.02867	83.08451	81.36475	81.6892751
95	100	51.42857		60.83451	64.93209	69.3565	65.65538	66.4285714
85	100	65.71429		70.76379	73.2671	74.99356	73.54934	73.6816448
85	100	75.71429		78.68458	80.30936	80.99957	80.42219	80.3582026
85	100	75.71429		78.68458	80.30936	80.99957	80.42219	80.3582026
90	100	64.28571		70.32532	73.12374	75.60704	73.5297	73.870284
70	100	70		72.07921	73.69718	73.15315	73.60825	73.115727
95	100	88.57143		90.2546	91.08903	91.66452	91.18311	91.2272149
85	100	77.14286		79.81612	81.31539	81.85757	81.40403	81.3119966
85	100	64.28571		69.63225	72.26107	74.13556	72.5675	72.7278508
60	100	61.42857		63.90382	65.93561	65.06221	65.79283	65.1080967
95	100	71.42857		76.6761	79.0166	81.36851	79.40108	79.7816872
90	100	74.28571		78.24611	80.166	81.61304	80.40255	80.5468419
70	100	35.71429		44.92221	49.55231	52.56113	50.04418	50.2246715
85	100	62.85714		68.50071	71.25503	73.27756	71.58567	71.7740568
80	100	45.71429		54.22914	58.31992	61.51008	58.84143	59.1860958
75	100	50		56.93069	60.47535	62.61261	60.82474	60.9050445

85	100	71.42857		75.28996	77.29125	78.42557	77.47668	77.4968207
90	100	81.42857		83.90382	85.19618	85.90305	85.31173	85.3158118
80	100	61.42857		66.6761	69.38632	70.94809	69.64163	69.6778296
85	100	65.71429		70.76379	73.2671	74.99356	73.54934	73.6816448
90	100	75.71429		79.37765	81.17203	82.47104	81.38439	81.5006359
90	100	81.42857		83.90382	85.19618	85.90305	85.31173	85.3158118
95	100	88.57143		90.2546	91.08903	91.66452	91.18311	91.2272149
90	100	84.28571		86.1669	87.20825	87.61905	87.27541	87.2233997
80	100	82.85714		83.64922	84.47686	83.8181	84.36917	83.9847393
65	100	58.57143		62.3338	64.78622	64.81767	64.79136	64.3429419
75	100	78.57143		79.56153	80.59608	79.77263	80.46146	79.9809241
90	100	87.14286		88.42999	89.22032	89.33505	89.23908	89.1309877
65	100	84.28571		82.70156	82.89487	80.26169	82.46441	81.5112336
90	100	90		90.69307	91.23239	91.05105	91.20275	91.0385757
85	100	85.71429		86.60537	87.35161	87.00558	87.29504	87.0347605
90	100	92.85714		92.95615	93.24447	92.76705	93.16642	92.9461636
75	100	90		88.61386	88.64437	86.63664	88.31615	87.611276
95	100	95.71429		95.91231	96.11922	95.95453	96.09229	95.9961848
85	100	80		82.07921	83.32746	83.57357	83.3677	83.2195846
75	100	90		88.61386	88.64437	86.63664	88.31615	87.611276
90	100	90		90.69307	91.23239	91.05105	91.20275	91.0385757
95	100	87.14286		89.12306	90.083	90.80652	90.20128	90.2734209
95	100	82.85714		85.72843	87.06489	88.23252	87.25577	87.412039
80	100	77.14286		79.12306	80.45272	80.3861	80.44183	80.1695634
70	100	65.71429		68.68458	70.67907	70.57915	70.66274	70.2543451
85	100	61.42857		67.36917	70.24899	72.41956	70.60383	70.8202628
90	100	71.42857		75.98303	78.15392	79.89704	78.43888	78.6392539
95	100	81.42857		84.59689	86.05885	87.37452	86.27393	86.458245
90	100	71.42857		75.98303	78.15392	79.89704	78.43888	78.6392539
95	100	77.14286		81.20226	83.04074	84.80051	83.32842	83.5968631
65	100	58.57143		62.3338	64.78622	64.81767	64.79136	64.3429419
65	100	72.85714		73.64922	74.84658	73.39768	74.60972	73.8808817
80	100	54.28571		61.01839	64.35614	66.65809	64.73245	64.9088597
85	100	50		58.31683	62.2007	65.55556	62.74914	63.189911
60	100	58.57143		61.64074	63.92354	63.3462	63.82916	63.2005087
70	100	75.71429		76.60537	77.72133	76.58516	77.53559	76.9309029
70	100	77.14286		77.73692	78.72736	77.44316	78.51743	77.8846969
90	100	74.28571		78.24611	80.166	81.61304	80.40255	80.5468419
65	100	48.57143		54.41301	57.74396	58.81167	57.91851	57.6663841
85	100	75.71429		78.68458	80.30936	80.99957	80.42219	80.3582026
90	100	80		82.77228	84.19014	85.04505	84.3299	84.3620178
80	100	70		73.46535	75.42254	76.0961	75.53265	75.4005935
75	100	78.57143		79.56153	80.59608	79.77263	80.46146	79.9809241
85	100	82.85714		84.34229	85.33954	85.28958	85.33137	85.1271725
95	100	78.57143		82.3338	84.04678	85.65852	84.31026	84.5506571

95	100	55.71429		64.22914	67.9502	71.9305	68.60088	69.2899534
80	100	75.71429		77.99151	79.44668	79.5281	79.45999	79.2157694
90	100	74.28571		78.24611	80.166	81.61304	80.40255	80.5468419
80	100	62.85714		67.80764	70.39235	71.80609	70.62347	70.6316236
85	100	74.28571		77.55304	79.30332	80.14157	79.44035	79.4044086
95	100	85.71429		87.99151	89.07696	89.94852	89.21944	89.319627
85	100	68.57143		73.02687	75.27918	76.70957	75.51301	75.5892327
70	100	48.57143		55.10608	58.60664	60.28314	58.88071	58.8088173
90	100	57.14286		64.66761	68.09356	71.31703	68.62052	69.1013141
80	100	60		65.54455	68.38028	70.09009	68.65979	68.7240356
75	100	54.28571		60.32532	63.49346	65.18662	63.77025	63.7664265
80	100	74.28571		76.85997	78.44064	78.6701	78.47815	78.2619754
85	100	72.85714		76.4215	78.29728	79.28357	78.45852	78.4506147
60	100	60		62.77228	64.92958	64.2042	64.811	64.1543027
65	100	42.85714		49.88685	53.71982	55.37967	53.99116	53.8512081
80	100	64.28571		68.93918	71.39839	72.66409	71.6053	71.5854175
60	100	65.71429		67.29844	68.95372	67.63621	68.73834	67.9694786
80	100	50		57.62376	61.33803	64.08408	61.78694	62.0474777
90	100	52.85714		61.27298	65.07545	68.74303	65.67501	66.2399322
75	100	68.57143		71.64074	73.55382	73.76662	73.58861	73.3043663
80	100	70		73.46535	75.42254	76.0961	75.53265	75.4005935
85	100	75.71429		78.68458	80.30936	80.99957	80.42219	80.3582026
45	100	71.42857		69.7454	70.38984	66.6538	69.77909	68.3573548
65	100	60		63.46535	65.79225	65.67568	65.7732	65.2967359
80	100	65.71429		70.07072	72.40443	73.52209	72.58714	72.5392115
70	100	71.42857		73.21075	74.70322	74.01115	74.59008	74.069521
70	100	58.57143		63.02687	65.64889	66.28915	65.75356	65.4853752
85	100	85.71429		86.60537	87.35161	87.00558	87.29504	87.0347605
55	100	67.14286		67.73692	69.09708	67.02274	68.75798	67.7808393
90	100	82.85714		85.03536	86.20221	86.76105	86.29357	86.2696058
80	100	87.14286		87.04385	87.49497	86.39211	87.31468	86.8461212
75	100	42.85714		51.27298	55.44517	58.32261	55.91556	56.1360746
85	100	54.28571		61.71146	65.21881	68.12956	65.69465	66.0512929
70	100	50		56.23762	59.61268	61.14114	59.86254	59.7626113
90	100	87.14286		88.42999	89.22032	89.33505	89.23908	89.1309877
65	100	75.71429		75.91231	76.85865	75.11369	76.57339	75.7884697
70	100	80		80	80.73944	79.15916	80.4811	79.7922849
65	100	35.71429		44.22914	48.68964	51.08966	49.08198	49.0822382
65	100	62.85714		65.72843	67.80433	67.39168	67.73687	67.2043239
75	100	74.28571		76.1669	77.57797	77.19863	77.51595	77.1195422
65	100	54.28571		58.93918	61.76811	62.24367	61.84585	61.48156
80	100	67.14286		71.20226	73.41046	74.38009	73.56897	73.4930055
75	100	65.71429		69.37765	71.54175	72.05062	71.62494	71.3967783
85	100	80		82.07921	83.32746	83.57357	83.3677	83.2195846
65	100	67.14286		69.12306	70.82243	69.96568	70.68238	70.0657058
60	100	80		78.61386	79.01408	76.21622	78.5567	77.5074184

60	100	58.57143		61.64074	63.92354	63.3462	63.82916	63.2005087
75	100	68.57143		71.64074	73.55382	73.76662	73.58861	73.3043663
95	100	78.57143		82.3338	84.04678	85.65852	84.31026	84.5506571
75	100	72.85714		75.03536	76.57193	76.34063	76.53412	76.1657482
75	100	35.71429		45.61528	50.41499	54.0326	51.00638	51.3671047
90	100	72.85714		77.11457	79.15996	80.75504	79.42072	79.5930479
95	100	67.14286		73.28147	75.99849	78.79451	76.45557	76.9203052
65	100	44.28571		51.01839	54.72586	56.23767	54.973	54.8050021
65	100	60		63.46535	65.79225	65.67568	65.7732	65.2967359
80	100	57.14286		63.28147	66.36821	68.37409	66.69612	66.8164476
65	100	58.57143		62.3338	64.78622	64.81767	64.79136	64.3429419
60	100	60		62.77228	64.92958	64.2042	64.811	64.1543027
70	100	67.14286		69.81612	71.68511	71.43715	71.64458	71.208139
85	100	68.57143		73.02687	75.27918	76.70957	75.51301	75.5892327
70	100	58.57143		63.02687	65.64889	66.28915	65.75356	65.4853752
75	100	72.85714		75.03536	76.57193	76.34063	76.53412	76.1657482
85	100	70		74.15842	76.28521	77.56757	76.49485	76.5430267
80	100	41.42857		50.83451	55.30181	58.93608	55.89593	56.3247139
75	100	68.57143		71.64074	73.55382	73.76662	73.58861	73.3043663
75	100	68.57143		71.64074	73.55382	73.76662	73.58861	73.3043663
75	100	44.28571		52.40453	56.45121	59.18061	56.8974	57.0898686
75	100	77.14286		78.42999	79.59004	78.91463	79.47963	79.0271301
60	100	51.42857		55.98303	58.89336	59.0562	58.91998	58.4315388
85	100	61.42857		67.36917	70.24899	72.41956	70.60383	70.8202628
85	100	67.14286		71.89533	74.27314	75.85157	74.53117	74.6354387
90	100	61.42857		68.06223	71.11167	73.89103	71.56603	71.9626961
75	100	48.57143		55.79915	59.46932	61.75461	59.84291	59.9512505
80	100	62.85714		67.80764	70.39235	71.80609	70.62347	70.6316236
85	100	57.14286		63.97454	67.23089	69.84556	67.65832	67.9588809
90	100	51.42857		60.14144	64.06942	67.88503	64.69318	65.2861382
90	100	54.28571		62.40453	66.08149	69.60103	66.65685	67.1937262
95	100	71.42857		76.6761	79.0166	81.36851	79.40108	79.7816872
55	100	67.14286		67.73692	69.09708	67.02274	68.75798	67.7808393
55	100	58.57143		60.94767	63.06087	61.87473	62.86696	62.0580755
65	100	35.71429		44.22914	48.68964	51.08966	49.08198	49.0822382
55	100	64.28571		65.47383	67.08501	65.30674	66.79431	65.8732514
65	100	51.42857		56.6761	59.75604	60.52767	59.88218	59.573972
75	100	50		56.93069	60.47535	62.61261	60.82474	60.9050445
90	100	57.14286		64.66761	68.09356	71.31703	68.62052	69.1013141
85	100	61.42857		67.36917	70.24899	72.41956	70.60383	70.8202628
55	100	27.14286		36.05375	40.92807	42.99871	41.26657	41.0746079
60	100	22.85714		33.35219	38.77264	41.89618	39.28326	39.3556592
90	100	55.71429		63.53607	67.08753	70.45903	67.63868	68.1475201
60	100	64.28571		66.1669	67.94769	66.77821	67.7565	67.0156846
95	100	70		75.54455	78.01056	80.51051	78.41924	78.8278932
60	100	41.42857		48.06223	51.85111	53.05019	52.04713	51.7549809

75	100	51.42857		58.06223	61.48139	63.47061	61.80658	61.8588385
80	100	70		73.46535	75.42254	76.0961	75.53265	75.4005935
80	100	61.42857		66.6761	69.38632	70.94809	69.64163	69.6778296
75	100	78.57143		79.56153	80.59608	79.77263	80.46146	79.9809241
70	100	72.85714		74.34229	75.70926	74.86915	75.57192	75.023315
65	100	65.71429		67.99151	69.8164	69.10768	69.70054	69.1119118
70	100	64.28571		67.55304	69.67304	69.72115	69.6809	69.3005511
80	100	77.14286		79.12306	80.45272	80.3861	80.44183	80.1695634
70	100	70		72.07921	73.69718	73.15315	73.60825	73.115727
95	100	54.28571		63.0976	66.94416	71.0725	67.61905	68.3361594
80	100	77.14286		79.12306	80.45272	80.3861	80.44183	80.1695634
85	100	80		82.07921	83.32746	83.57357	83.3677	83.2195846
65	100	38.57143		46.49222	50.70171	52.80566	51.04566	50.9898262
90	100	70		74.85149	77.14789	79.03904	77.45704	77.6854599
90	100	64.28571		70.32532	73.12374	75.60704	73.5297	73.870284
70	100	47.14286		53.97454	57.6006	59.42514	57.89887	57.8550233
75	100	50		56.93069	60.47535	62.61261	60.82474	60.9050445
70	100	45.71429		52.843	56.59457	58.56714	56.91703	56.9012293
80	100	70		73.46535	75.42254	76.0961	75.53265	75.4005935
70	100	62.85714		66.4215	68.667	68.86315	68.69907	68.3467571
50	100	14.28571		25.1768	31.01107	33.80523	31.46784	31.3480288
70	100	67.14286		69.81612	71.68511	71.43715	71.64458	71.208139
65	100	70		71.38614	72.83451	71.68168	72.64605	71.9732938
70	100	62.85714		66.4215	68.667	68.86315	68.69907	68.3467571
80	100	54.28571		61.01839	64.35614	66.65809	64.73245	64.9088597
90	100	52.85714		61.27298	65.07545	68.74303	65.67501	66.2399322
60	100	58.57143		61.64074	63.92354	63.3462	63.82916	63.2005087
80	100	68.57143		72.3338	74.4165	75.2381	74.55081	74.4467995
65	100	51.42857		56.6761	59.75604	60.52767	59.88218	59.573972
75	100	68.57143		71.64074	73.55382	73.76662	73.58861	73.3043663
50	100	47.14286		51.20226	54.1499	53.53925	54.05007	53.2852904
60	100	44.28571		50.32532	53.86318	54.76619	54.0108	53.6625689
50	100	37.14286		43.28147	47.10765	47.53325	47.17722	46.6087325
80	100	71.42857		74.59689	76.42857	76.9541	76.51448	76.3543875
75	100	70		72.77228	74.55986	74.62462	74.57045	74.2581602
85	100	78.57143		80.94767	82.32143	82.71557	82.38586	82.2657906
45	100	48.57143		51.64074	54.29326	52.92578	54.06971	53.0966511
65	100	67.14286		69.12306	70.82243	69.96568	70.68238	70.0657058
90	100	82.85714		85.03536	86.20221	86.76105	86.29357	86.2696058
80	100	52.85714		59.88685	63.3501	65.80009	63.75061	63.9550657
90	100	65.71429		71.45686	74.12978	76.46504	74.51154	74.824078
75	100	57.14286		62.5884	65.50553	66.90262	65.73392	65.6740144
70	100	38.57143		47.18529	51.56439	54.27713	52.00785	52.1322594
40	100	35.71429		40.76379	44.37626	43.7323	44.27099	43.3700721
95	100	71.42857		76.6761	79.0166	81.36851	79.40108	79.7816872

Topics Beyond The syllabus

Advanced CMOS Technologies:

FinFET and Nanoscale Transistors: Explore advanced transistor technologies such as FinFETs and nanoscale transistors, which are crucial in modern VLSI design due to their improved performance and energy efficiency.

Analog and Mixed-Signal Design:

Operational Amplifiers (Op-Amps): Study the design and analysis of operational amplifiers, which are essential components in analog and mixed-signal ICs.

Data Converters: Learn about the design of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) used in various applications, including communication and sensor interfaces.

Custom IC Design:

Custom IC Layout: Dive deeper into custom IC layout and design techniques, including analog layout design and mixed-signal IC layout.

Memory Design:

SRAM and DRAM Design: Explore the design principles of static random-access memory (SRAM) and dynamic random-access memory (DRAM) cells, which are fundamental in memory design.

Design for Testability (DFT):

Built-In Self-Test (BIST): Understand BIST techniques for testing and diagnosing ICs during manufacturing and in the field.

Scan Chains: Learn about scan chain design and how it helps with testing and debugging complex ICs.

System-on-Chip (SoC) Design:

SoC Architecture: Explore the architecture and design principles of complex SoCs, which integrate multiple components, including processors, memory, and peripherals on a single chip.

Digital Design Automation:

EDA Tools and Flows: Get insights into Electronic Design Automation (EDA) tools and design flows used for IC design and verification.**:**

R G M COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

Department of Electronics and Communication Engineering

Academic Year-2022-23

Subject: VLSID

Expert suggestions

Online Courses and Tutorials: Enroll in online courses or watch tutorials on platforms like Coursera, edX, or YouTube to supplement your knowledge in specific areas of interest.

Hands-On Projects: Undertake hands-on projects to apply what you've learned. Consider designing simple ICs or creating digital and analog circuits on breadboards or using simulation software like SPICE.

Internships: Look for internships at semiconductor companies or IC design firms. Practical experience is highly valuable, and it can also help you build a professional network.

Student Clubs and Competitions: Join IC design or electronics-related student clubs or participate in design competitions. These experiences can enhance your practical skills and provide exposure to real-world problems.

Academic Research: If you're at an academic institution, explore opportunities to engage in research projects related to IC design under the guidance of professors or researchers.

Signature of the subject Expert

Dr.A.Sathish,

Professor,ECE Dept.

RGMCET

Assessment

Rajeev Gandhi Memorial College of Engineering & Technology
(Autonomous Institution | Approved by AICTE New Delhi | Affiliated to JNTU Anantapur)
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S.No.	Year (Batch)	Section	Subject	Branch	Registered	Appeared	Failed	Pass(%)	Highest
1	II B.Tech. II Sem. & 2021	D	ECAD Lab	ECE	70	68	5	92.65	10
2	II B.Tech. II Sem. & 2021	D	ECAD	ECE	70	68	22	67.65	9
3	IV B.Tech. II Sem. & 2019	B	SEM	ECE	70	70	0	100.00	10
4	II B.Tech. I Sem. & 2021	D	EDC Lab	ECE	74	61	4	93.44	10
5	IV B.Tech. I Sem. & 2019	D	VLSID	ECE	62	62	6	90.32	9
6	IV B.Tech. I Sem. & 2019	A	VLSID	ECE	70	70	0	100.00	10
7	II B.Tech. I Sem. & 2020	B	EDC Lab	ECE	66	61	4	93.44	10
8	IV B.Tech. I Sem. & 2018	D	VLSI	ECE	60	55	4	92.73	9
9	IV B.Tech. I Sem. & 2018	A	VLSI	ECE	67	67	0	100.00	10
10	III B.Tech. II Sem. & 2018	D	MPMC Lab	ECE	60	60	0	100.00	10
11	III B.Tech. II Sem. & 2018	D	MPMC	ECE	60	55	15	72.73	9
12	III B.Tech. I Sem. & 2018	A	DICA V&V Lab	ECE	68	68	0	100.00	10
13	III B.Tech. I Sem. & 2018	D	DICA VHDL	ECE	62	58	18	68.97	9
14	III B.Tech. I Sem. & 2018	A	DICA VHDL	ECE	68	68	0	100.00	10
15	III B.Tech. II Sem. & 2017	A	MPMC Lab	ECE	57	56	0	100.00	10
16	III B.Tech. II Sem. & 2017	A	MPMC	ECE	57	57	0	100.00	9
17	III B.Tech. I Sem. & 2017	D	DICA V&V Lab	ECE	50	50	0	100.00	10
18	III B.Tech. I Sem. & 2017	D	DICA VHDL	ECE	50	50	1	98.00	10
19	III B.Tech. I Sem. & 2017	C	DICA VHDL	ECE	55	52	0	100.00	10
20	III B.Tech. II Sem. & 2016	C	MPMC Lab	ECE	56	54	1	98.15	10
21	III B.Tech. II Sem. & 2016	C	MPMC	ECE	56	55	4	92.73	10
22	III B.Tech. I Sem. & 2016	B	DICA V&V Lab	ECE	56	52	2	96.15	10

S.No.	Year (Batch)	Section	Subject	Branch	Registered	Appeared	Failed	Pass(%)	Highest
23	IV B.Tech. I Sem. & 2015	D	VLSI	ECE	59	59	0	100.00	10
24	IV B.Tech. I Sem. & 2015	B	VLSI	ECE	60	60	2	96.67	10
25	III B.Tech. II Sem. & 2015	A	MPMC Lab	ECE	64	62	0	100.00	10
26	III B.Tech. II Sem. & 2015	B	MPMC	ECE	60	59	1	98.31	10
27	III B.Tech. II Sem. & 2015	A	MPMC	ECE	64	64	1	98.44	10
28	III B.Tech. I Sem. & 2015	A	DICA V&V Lab	ECE	64	63	2	96.83	10
29	III B.Tech. I Sem. & 2015	A	DICA VHDL	ECE	64	63	4	93.65	9
30	III B.Tech. II Sem. & 2014	B	DICA V& V Lab	ECE	69	69	0	100.00	71
31	M.Tech. II Sem. & 2016	A	DFTS	DSCE	1	1	0	100.00	8
32	III B.Tech. II Sem. & 2014	B	ME VLSID	ECE	69	69	2	97.10	91
33	III B.Tech. I Sem. & 2014	C	MP& MC	ECE	67	65	0	100.00	73
34	III B.Tech. I Sem. & 2014	B	MP& MC	ECE	69	69	2	97.10	73
35	III B.Tech. I Sem. & 2014	C	MP& MC	ECE	67	64	7	89.06	84